Project Report
A 5.2 GHz Differential Cascode Low Noise Amplifier
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April 2, 2004

ELEC 4907 – Fourth Year Engineering Project

Final Report

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Abstract

As the demand for wireless network access increases so does the need for high performance wireless Local Area Network (LAN) transceivers. One of the key components of the wireless LAN transceiver is the Low-Noise Amplifier (LNA).

In this report, the design of a LNA to meet specifications is explained. The circuit was built using the IBM sige5am bipolar process along with Cadence as a CAD tool. Simulations using Cadence allowed the LNA to be optimized for better performance. With the LNA designed, the physical layout of the amplifier was performed using Cadence. The layout was performed to witness the effect of physical layout on the LNA's operation.

The design of the LNA was simulated in Cadence to verify its performance. In most cases, the objectives of the project were met. However, recommendations for further research and work are outlined in this report. The future work can be divided into work on the circuit design, the integration of the LNA in a transceiver and development of layout.

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1.0 Introduction

The purpose of this project was the design of a Low Noise Amplifier (LNA) at 5.2 GHz for wireless Local Area Network (LAN) applications. The LNA was designed to meet specifications that were set to ensure that the LNA would be able to operate in a complete receiver.

The field of Radio Frequency Integrated Circuit (RFIC) design is a growing one as a result of increased demand for wireless products. LNAs are an essential part of wireless LAN transceivers and as their demand increases so does the requirements for better performance. Some pressing issues in the design of narrowband LNAs include the linearity of the amplifier, noise added to the system by the amplifier and the quality of integrated inductors.

The objectives of the project were:

a) to learn the RFIC design process
b) to design a LNA to meet specifications
c) to gain experience using CAD tools to build and simulate the LNA
d) work as part of an engineering team

This document provides background information and describes the tools used to build the LNA. As well, it explains the design methodology of the LNA and provides and explains simulation results. The layout process is discussed in this paper. Finally, recommendations for others working on similar projects and for possible future work are provided.

2.0 Background Information

In this section of the report, background information concerning the project will be provided.

2.1 Wireless LAN Transceivers

The prominence of wireless LANs is increasing as the public begins to realize the benefits of wireless access to networks have in the workplace, at home and in public areas. At the heart of wireless LANs is the transceiver which allows the data to be transmitted. The transceiver transmits and receives data while ensuring that the data is not lost as it is transmitted.

A simplified diagram of a Radio Frequency (RF) transceiver is shown below (Fig. 1). The antenna receives the input signal which is then filtered by a bandpass filter to ensure only the desired band is processed. The signal is then fed into the LNA which amplifies it. The image reject filter blocks any signals that may be mixed down and produce any distortion of the desired signal. The mixer down converts the RF signal to the Intermediate Frequency (IF) which then can be processed in the receiver's backend. The mixer uses a local oscillator frequency produced by a voltage controlled oscillator to down convert the RF signal to the IF. With the signal down-converted to the IF the signal can be processed in the baseband.

In the transmit side, signals are modulated in the baseband and IF stages and up-converted by the mixer which uses a Voltage-Controlled Oscillator (VCO). The up-converted signal is amplified to transmission by the power amplifier. As a result of improved efficiency the power amplifier is usually non-linear and produces many harmonics. The low-pass filter is used to filter out the harmonics for transmission by the antenna [1].

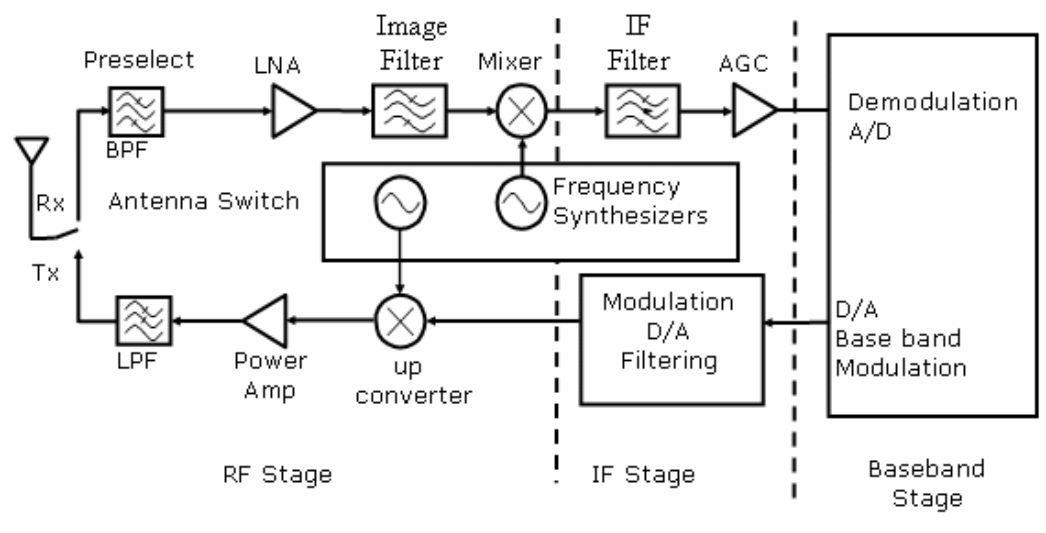

Figure 1: Simplified block diagram of receiver end of radio

2.2 Specifications & Design Tools

To design the LNA, an IBM sige5am, 2.5 μm, 50 GHz bipolar process was used. For this process the minimum length of the transistor's emitter is 2.5 μm and during the layout process 4 levels of metal are available. A bipolar process was chosen over CMOS since BJTs have improved noise and speed performance. As well, the models for CMOS at radio frequencies are not clearly defined and therefore tend to cause design to be more difficult [2]. Cadence was used as a CAD tool and layout tool.

Specifications, as laid out in Table 1, were outlined through consultations with Dr. Rogers. The specifications outline the requirements for LNA.

Parameter	Specification
Voltage Gain	15-20 dB
Centre frequency	5.2 GHz
Minimum bandwidth	200 MHz
Noise Figure	≤ 3 dB
Third-Order Intercept Point	≥ -20 dBm
Supply Voltage	3 V
DC Current	≤ 20 mA

Table 1: LNA Specifications

These specifications ensure that the LNA will provide sufficient gain with minimum noise added while maintaining linearity.

2.3 Group Members

Each group member designed a component of the transceiver. In the table below, group members and the components they designed are shown.

Andre Williams	5.2 GHz Colpitts Common Base Oscillator
Susan Yuen	2.4 GHz Differential Cascode LNA
Kenneth Ng	5.2 GHz Power Amplifier
Tarun Patel	Broadband LNA
Hao Shan	5.2 GHz Power Amplifier

Table 2: Group members and components designed

3.0 Low Noise Amplifier Theory

This section will outline the purpose of the LNA. As well, important factors in the design of the LNA will be explained.

3.1 Introduction

The input signals into the RF receiver are usually weak signals. Therefore, the LNA's principal purpose is to amplify weak signals. However, the LNA must not add significant amounts of noise as noise limits how weak a signal can be for processing. Noise will be a driving concern in the LNA so that other components in the receiver do not have to be designed with noise as a major concern. Since the system will be receiving data, linearity is a concern so that the integrity of the information is maintained. Linearity will cause distortion which could result in the data being corrupted. As well, linearity limits how large a signal can be [1].

3.2 Noise

Noise is present in any electrical system and is added by several sources. At higher frequencies, the random movement of electrons is a main source of noise in a system. In integrated circuits, noise is amplified by amplifiers and added by the random movement of electrons in resistors, across junctions in transistors among other factors [2]. A common measure of noise added to the system by the circuitry is the noise factor (F) which, if measured in decibels, is known as the Noise Figure (NF).

$$F = \frac{(S/N)_{IN}}{(S/N)_{OUT}} = \frac{GN_{IN} + N_{added}}{GN_{IN}}$$

where: (S/N) is the signal to noise ratio

G is the gain of the circuit

and N_{added} is the noise added by the circuit

$$NF = 10\log(F)$$

3.3 Linearity

Ideally, the output of a circuit is linearly related to the input. In a real circuit, the gain is not linear as a result of devices, power supply rails, etc. [2]. The nonlinear circuit's output voltage can be described in the following power series:

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^{\ 2} + k_3 v_{in}^{\ 3} + \ldots$$

With v_{in} as a function of two sinusoidal signals: $v_{in} = x_1 + x_2 = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$

Substituting into v_{out}:

$$v_{out} = k_0 + k_1(x_1 + x_2) + k_2(x_1 + x_2)^2 + k_3(x_1 + x_2)^3 + \ldots$$

$$v_{out} = k_0 + \underbrace{k_1(x_1 + x_2)}_{Fundamental} + \underbrace{k_2\left(x_1^{\ 2} + 2x_1x_2 + x_2^{\ 2}\right)}_{2^{nd}\ Order} + \underbrace{k_3\left(x_1^{\ 3} + 3x_1^{\ 2}x_2 + 3x^1x_2^{\ 2} + x_2^{\ 3}\right)}_{3^{rd}\ Order} + \ldots$$

where: $x_1^{\ 2}$ and $x_2^{\ 2}$ are composed of DC and second harmonic terms

$2x_1x_2$ is the second-order intermodulation term

$x_1^{\ 3}$ is composed of the fundamental and third harmonic terms

$3x_1^{\ 2}x_2$ and $3x_1^{\ 1}x_2^{\ 2}$ are composed of third-order intermodulation and fundamental terms

The third-order intermodulation terms are undesired since they produce nonlinearity such as intermodulation distortion and gain compression. As well, they are difficult to filter as they are usually in the desired band. [2]

4.0 Design Methodology

In this section, the steps taken to design the LNA are explained. The topology of the LNA is examined first, followed by a discussion on biasing the transistors. Input matching is also discussed along with output buffers and differential amplifiers. Finally, the sizing of the components is discussed.

4.1 Amplifier Theory

The three basic amplifier configurations for bipolar transistors are shown in Figure 2. The common-emitter (CE) amplifier provides reasonable voltage gain and input and output impedance however it suffers from limited bandwidth. The common-base (CB) amplifier has a reasonable output impedance and voltage gain as well as high bandwidth but it's input impedance tends to be fairly low (approximately 25 Ω at 1 mA.) The common-collector (CC) amplifier has high bandwidth and sufficient input impedance however it has a voltage gain of approximately 1. [3]

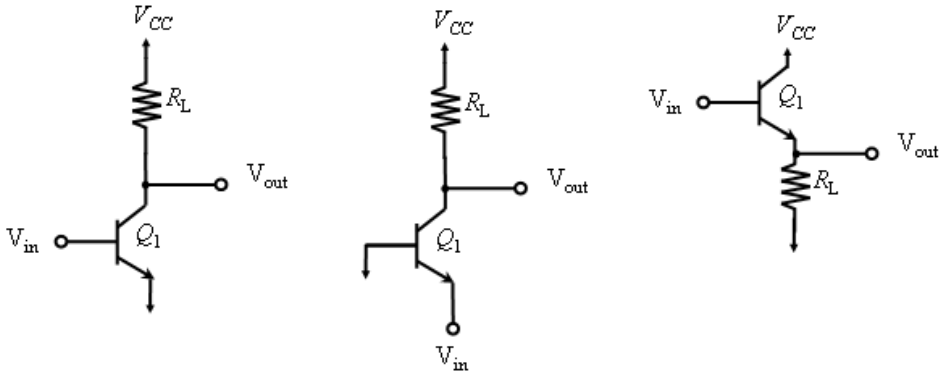

Figure 2: Common-emitter, common-base and common-collector amplifiers

The simplified small signal model of the high frequency bipolar transistor is shown in Figure 3. The capacitance, C_μ, can be simplified using Miller's Theorem, as a function of the gain across the two terminals of the small signal model.

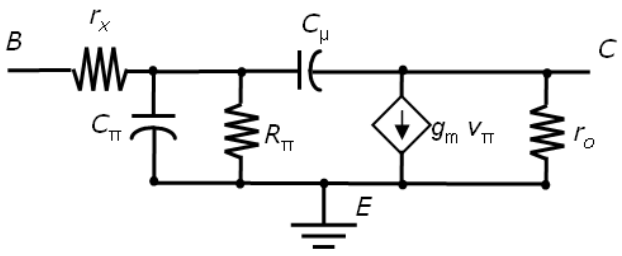

Figure 3: Simplified small signal model of the bipolar transistor

The cascode amplifier, as seen in Figure 4, is built with a CE amplifier, Q1, acting as the driver. With the addition of the CB amplifier, Q2, as the load of the CE, the frequency response is improved as the low input impedance of the CB increases the dominant pole frequency of the CE amplifier. However, the cascode amplifier must have a higher supply voltage since voltage must be shared [4]. As well, there is a reduced signal swing which can affect the linearity of the circuit.

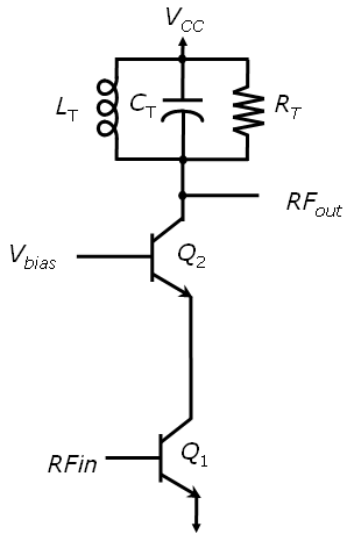

Figure 4: Cascode amplifier

4.2 Biasing

To ensure that the transistors operate in the forward active region, proper biasing of the transistors is required. The forward active region provides good gain and has improved linearity and noise performance. For the BJTs to be in the forward active region, V_C

must be greater than V_B and V_{BE} must be greater than the threshold voltage. In the case of the transistors used at 5.2 GHz, V_{BE} is approximately 0.9 V.

The use of a signal reference to bias the transistors ensures a dependable supply current independent of temperature. The current mirror, as shown in Figure 5, has a current reference as an input and produces a current N times greater than the current reference. The chosen configuration for the current mirror has one of the mirror transistors also acting as a driving transistor. As well, the input signal is inserted at the base of the driving transistor. However, the base resistance is large enough compared to the input impedance of the driving transistor which ensures that the input signal is fed into the driving transistor. The additional transistor ensures that the base current is not affected by loading of the transistor. The capacitor is able to reduce some of the noise created as a result of the high transconductance of the driving transistor [2].

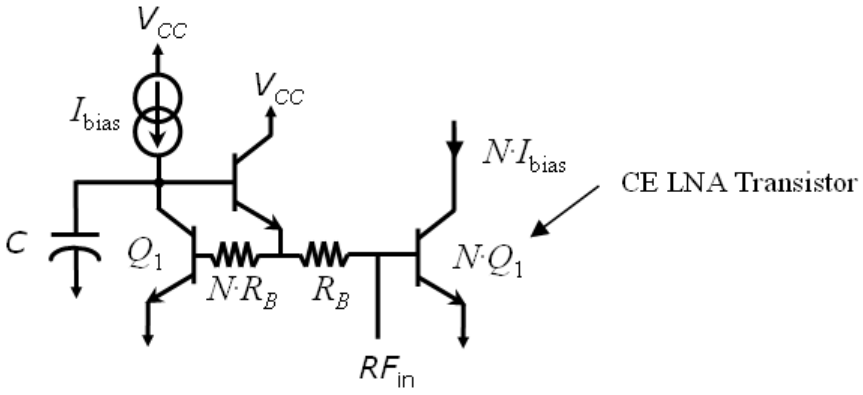

Figure 5: Current mirror used to bias transistors

Since ideal current sources are not available for integrated circuits, in the final circuit the ideal current source was replaced with a resistor, R_{ref}. The disadvantages of using a resistor are that it will add to the noise of the system and will be temperature dependent.

The common-base transistor of the cascode amplifier can be biased by using a resistor network as shown in Figure 6. The resistor network was designed to ensure that V_{B2} was less than V_{C2} and 0.9 V above V_{E2}. The resistor network was calculated as shown below. as follows:

$$R_1 = \frac{V_{CC} - V_{B2}}{10 I_B}$$

$$R_1 = \frac{V_{CC} - V_{B2}}{10 I_C \frac{I_C}{\beta}}$$

$$R_1 = \frac{(3V) - (2.65V)}{10 \frac{(4mA)}{(100)}}$$

$$R_1 = 875\Omega$$

$$V_{B2} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_{B2}(R_1 + R_2) = R_2 V_{CC}$$

$$R_2 = \frac{V_{B2} R_1}{V_{CC} - V_{B2}}$$

$$R_2 = \frac{(2.65V)(875\Omega)}{(3V) - (2.65V)}$$

$$R_2 = 6.625k\Omega$$

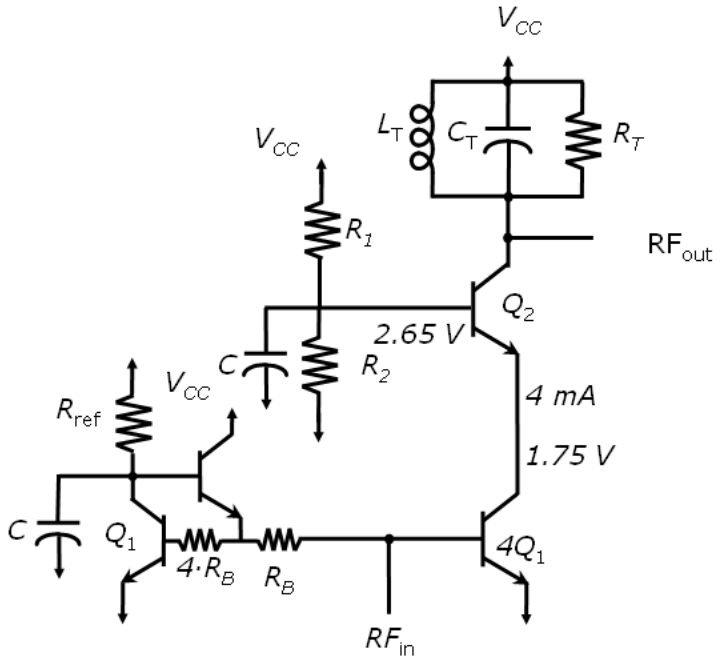

Figure 6: Cascode transistor showing current mirror and resistor network

4.3 Tuned Tank

A tuned tank was inserted at the collector of the output stage of the cascode. The tuned tank acts as a filter to ensure that the specifications for centre frequency, bandwidth and gain were met. A capacitance of 1 pF was chosen which results in an inductor of 937 pH, as shown below. However, once real components were added to the circuit, the inductor and capacitor values had to be slightly changed to meet the specifications.

$$\omega_o = \frac{1}{\sqrt{L_T C_T}}$$

$$L_T = \frac{1}{C_T \omega_o^{\,2}}$$

$$L_T = \frac{1}{(1pF)(2\pi \times 5.2 \times 10^9 rad/s)^2}$$

$$L_T \cong 936.78 pH$$

However, the inductor will have some resistance. The resistance can be modeled as a resistor in parallel, as shown below.

$$r_p = \omega_o L Q$$

$$r_p = (2\pi \times 5.2 \times 10^9 rad/s)(936.78 pH)(50) \quad \text{Assuming Q = 50}$$

$$r_p \cong 1.53 k\Omega$$

Using a simplifier equation for the gain of the cascode amplifier at 5.2 GHz, the required load resistance can be calculated. This equation is valid as long as Z_π is capacitive at 5.2 GHz and the input is matched – matching will be performed later.

$$|\frac{v_{out}}{v_{in}}|=\frac{g_m R_L}{R_S \omega_o C_\pi}$$

$$R_L=\frac{|\frac{v_{out}}{v_{in}}| R_S \omega_o C_\pi}{g_m}$$

Set the gain to 20 dB = 10 V/V

$$R_L=\frac{(10)(50\Omega)(2\pi\times 5.2\times 10^9 rad/s)(407 fF)}{(0.16)}$$

$$R_L \cong 207.8\Omega$$

With the load resistance calculated, the resistance required for the tuned tank can be found as follows:

$$R_L = R_T \,||\, r_p$$

$$\frac{1}{R_T}=\frac{1}{R_L}-\frac{1}{r_p}$$

$$\frac{1}{R_T}=\frac{1}{(207.8\Omega)}-\frac{1}{(1.53k\Omega)}$$

$$R_T \cong 240\Omega$$

The expected bandwidth can be calculated using the load resistance and the tuned tank capacitor.

$$BW=\frac{1}{R_L C}$$

$$BW=\frac{1}{(207.8\Omega)(1pF)}$$

$$BW \cong 766MHz$$

Obviously, the bandwidth is wide. The bandwidth can be decreased by decreasing R_L at the expense of gain.

4.4 Input Matching

To improve the LNA's performance in terms of gain, noise and power transfer, input matching was performed. Two inductors, one connected to the base and another to the emitter of the driver transistor as shown in Figure 7, can achieve simultaneous noise and power matching. The first step of matching was to find the current density that would ensure the lowest minimum noise figure. With the current density set, the emitter length was chosen by sweeping the emitter lengths of the cascode transistors to find at which point the real part of the optimum source impedance for the lowest noise figure was equal to 50 Ω. The emitter length of the cascode transistors was set to 17.5 μm. The emitter degeneration inductor was sized to match the real part of the input impedance to 50 Ω. The base inductor was sized to lower the effect of the imaginary part of the input impedance. The required emitter inductor was calculated, as shown below, to be approximately 253.87 pH and the base inductor was calculated to be approximately 925.79 pH. However, through simulations these values were changed for proper impedance matching.

$$L_e = \frac{R_S C_\pi}{g_m} \qquad L_b = \frac{1}{C_\pi \omega^2} - \frac{R_S C_\pi}{g_m}$$

$$L_e = \frac{(50\Omega)(794.1fF)}{(156.4mA/V)} \qquad L_b = \frac{1}{(794.1fF)(2\pi \times 5.2\times 10^9 rad/s)^2} - (253.87pH)$$

$$L_e \cong 253.87pH \qquad L_b \cong 925.79pH$$

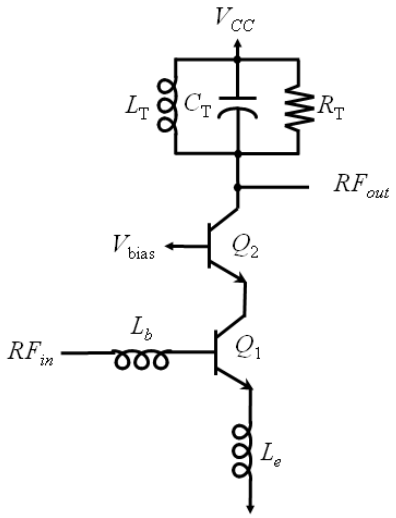

Figure 7: Cascode amplifier with inductors used for input matching

4.5 Output Buffer

To ensure that the LNA could be used to drive a mixer with high input impedance, an output buffer was added to the circuit, as shown in Figure 8. An emitter follower was used as the output buffer which will result in a voltage loss. The output buffer was designed to drive 50 Ω. A bias current of 3 mA from a current mirror was used to bias the output buffer. The output buffer transistor was sized to optimize noise performance and to minimize any losses.

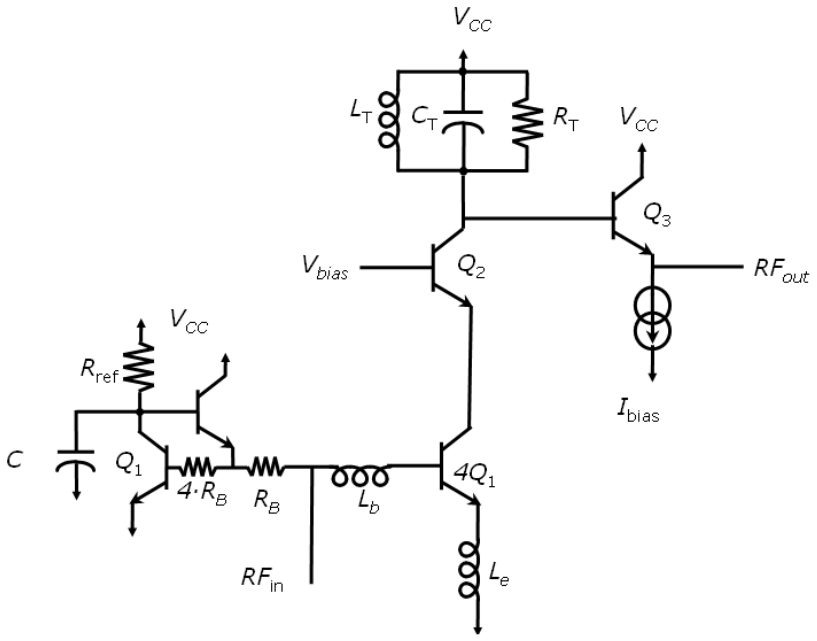

Figure 8: Simplified circuit showing output buffer and tuned tank

With emitter degeneration and output buffer incorporated into the circuit, the expected noise figure can be calculated. First, the noise voltage produced by the source resistance at the input must be calculated.

$$v_{ns} = \sqrt{4kTR_s}$$
$$v_{ns} = \sqrt{4\left(4\times10^{-21}\right)\left(50\Omega\right)}$$
$$v_{ns} \cong 894.4pV/\sqrt{Hz}$$

The noise voltage produced by the source resistance is divided between the input of the driver and the output since the input is matched. Therefore, the noise due to the source resistance at the output can be calculated as follows:

$$v_{o(source)} = \tfrac{1}{2} v_{ns} G$$
$$v_{o(source)} = \tfrac{1}{2}\left(894.4pV/\sqrt{Hz}\right)\left(10V/V\right)$$
$$v_{o(source)} \cong 4.47nV/\sqrt{Hz}$$

The current produced by the degeneration inductor can be calculated as:

$$i_{nE} = \sqrt{\frac{4kT}{R_E}}$$
$$i_{nE} = \sqrt{\frac{4\left(4\times10^{-21}\right)}{\left(13.2\Omega\right)}}$$
$$i_{nE} \cong 34.82\,pA/\sqrt{Hz}$$

The current generated by the emitter degeneration is divided between the inductor and the emitter of the driver. The amount of current that enters the driver produces a voltage at the collector of the cascode transistor and is passed through the follower to the output. [2] Although the buffer introduces losses, in the following calculation it is assumed that the buffer has unity gain.

$$v_{onE} = i_{nE}\left(\frac{R_E}{r_e + R_E}\right)R_L A_{buffer}$$
$$v_{onE} = \left(34.82\,pA/\sqrt{Hz}\right)\left(\frac{\left(13.2\Omega\right)}{\left(6\Omega\right)+\left(13.2\Omega\right)}\right)\left(207.8\Omega\right)(1)$$
$$v_{onE} \cong 4.97nV/\sqrt{Hz}$$

The noise figure can calculated simply as follows. It is assumed that the source resistance and the emitter degenerator are the two main noise sources. [2].

$$NF = 10\log\left(\frac{{v_{onE}}^2 + {v_{o(source)}}^2}{{v_{o(source)}}^2}\right)$$
$$NF = 10\log\left(\frac{\left(4.97nV/\sqrt{Hz}\right)^2 + \left(4.47nV/\sqrt{Hz}\right)^2}{\left(4.47nV/\sqrt{Hz}\right)^2}\right)$$
$$NF \cong 3.495dB$$

Therefore, the expected noise figure is 3.495 dB. Although this does not meet the specifications, during the simulation stage the performance of the LNA can be optimized.

4.6 Single Ended Amplifier

With the addition of the output buffer, the single ended amplifier topology was completed, as shown in Figure 9. Although all of the components had been calculated, simulations were performed to optimize the performance of the LNA. As well, real components were substituted for the ideal components. The real components introduced losses across the inductors. To minimize the losses in the inductors, the peak Q frequency was chosen to be slightly above the operating frequency of 5.2 GHz as Q falls rapidly past the peak frequency. All of the components were sized to ensure that their physical dimensions would be reasonable for integrated circuits. Once the real components were sized, simulations were performed and some of the components were altered to ensure that the LNA met the specifications.

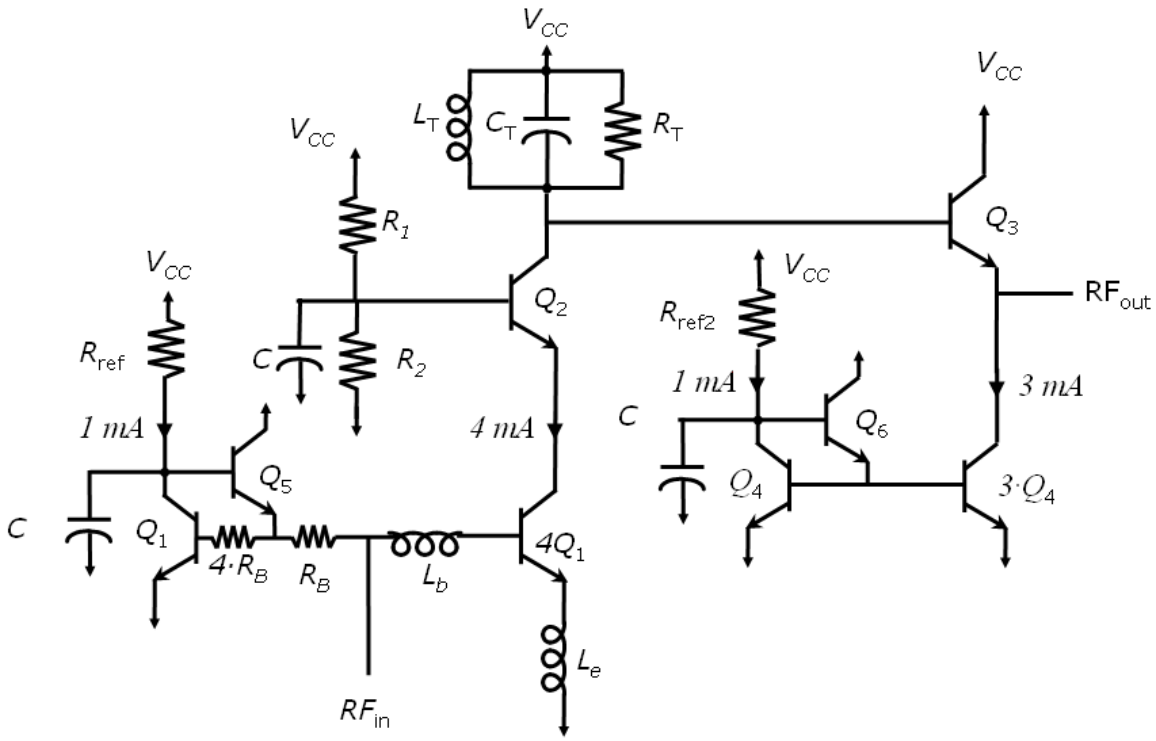

Figure 9: Single-ended LNA

In the tables below, the sizes and specifications of the components of the LNA are shown.

Parameters of component	Q1	4Q1	Q2	Q3	Q4	3Q4	Q5	Q6
Emitter length (μm)	17.5	17.5	17.5	15	17.5	17.5	20	20
Emitter width (nm)	500	500	500	500	500	500	500	500
Emitter area (pm^2)	8.72	8.72	8.72	7.25	8.72	8.72	10	10
Collector to emitter spacing (μm)	1.725	1.725	1.725	1.725	1.725	1.725	1.725	1.725
Multiplicity	1	4	1	1	1	3	1	1

Table 3: Transistor sizes

Parameters of component	Inductor L_T	Inductor L_b	Inductor L_e
Outer dimension (μm)	230	160	150
Am width (μm)	25	10	10
N turns	1.5	2.5	2
Max turns	2.5	2.5	2.5
Mt width (μm)	38	37.5	37.5
Space (μm)	5	5	5
Hollowness	0.560976	0.5	0.571429
Inductance (pH)	732.00	1.149	820
Simulation frequency (GHz)	5.4	6.4	8.2
Levels of metal	4	4	4
Ground plane	dt	dt	Dt

Table 4: Sizing of inductors

It should be noted that the two inductors L_e were placed in parallel since the calculated value for L_e was too small to be realized. Therefore, two copies of L_e were placed in parallel to meet the calculated inductance.