

# WireNet



## Gantt Chart

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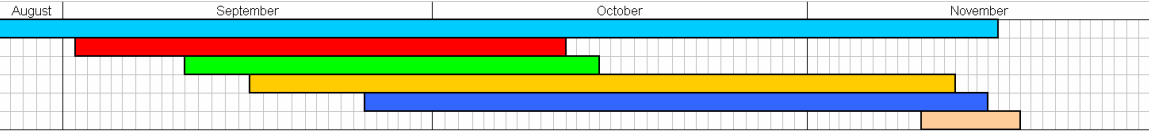


Figure 1. Gantt Chart Top Level.

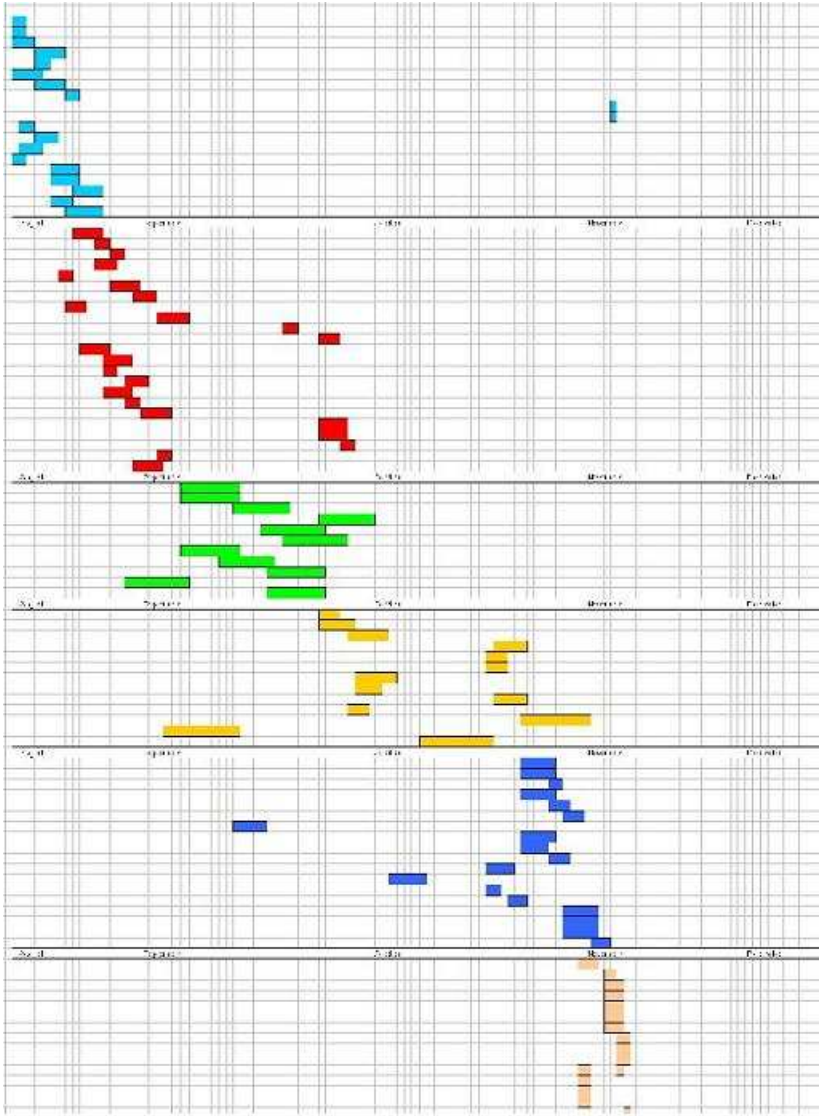


Figure 2. Overall Gantt Chart.

Table 1. Research Phase Gantt Tasks

Task Number	Task	Duration (days)	Start	Finish
Research Phase				
1.1.1.1.1	BPL Input Signal	2	27-Aug-07	28-Aug-07
1.1.1.1.2	BPL Output Signal	2	27-Aug-07	28-Aug-07
1.1.1.2	BPL Control Lines	3	27-Aug-07	29-Aug-07
1.1.1.2.1	BPL Chipset	4	30-Aug-07	2-Sep-07
1.1.1.2.2	Control Lines	2	30-Aug-07	31-Aug-07
1.1.2.2	uC Power Regulation	4	27-Aug-07	30-Aug-07
1.1.2.1	uC Input/Output	4	30-Aug-07	2-Sep-07
1.1.3	Power Supply	3	2-Sep-07	4-Sep-07
1.1.4.1	Prototype Cost	1	17-Nov-07	18-Nov-07
1.1.4.2	Mass Production Cost	1	17-Nov-07	18-Nov-07
1.2.1.1	IR Transmitter	2	28-Aug-07	29-Aug-07
1.2.1.2	Flash Memory	3	30-Aug-07	1-Sep-07
1.2.1.3	IR Driver	3	28-Aug-07	30-Aug-07
1.2.2	A/V IR Codes	2	27-Aug-07	28-Aug-07
1.3.1.1	Graphical Libraries (WireNet)	4	1-Sep-07	4-Sep-07
1.3.1.2	Logical Libraries	3	1-Sep-07	3-Sep-07
1.3.1.3	Software Structure	4	4-Sep-07	8-Sep-07
1.3.2.1	Logical Libraries (HECS)	3	1-Sep-07	3-Sep-07
1.3.2.2	Plugin System	5	3-Sep-07	7-Sep-07



Figure 3. Research Phase Gantt Chart.

Table 2. Design Phase Gantt Tasks.

Design Phase				
2.1.1.2	BPL Input/Output	4	4-Sep-07	7-Sep-07
2.1.1.1	BPL Power	2	7-Sep-07	8-Sep-07
2.1.1.3	BPL Coupling Transformer	2	9-Sep-07	10-Sep-07
2.1.2.1	uC Power	3	7-Sep-07	9-Sep-07
2.1.2.2	uC Input/Output	2	2-Sep-07	3-Sep-07
2.1.2.3	Ethernet to BPL chipset(802.3)	4	9-Sep-07	12-Sep-07
2.1.3	Power Supply	3	12-Sep-07	14-Sep-07
2.1.4	Flashable Boot Memory	3	3-Sep-07	5-Sep-07
2.1.5.1	WireNet Schematic	4	15-Sep-07	18-Sep-07
2.1.5.2	WireNet PCB Layout	2	2-Oct-07	3-Oct-07
2.1.5.3	WireNet Packaging	3	7-Oct-07	9-Oct-07
2.2.1	IR Adapter port	4	5-Sep-07	8-Sep-07
2.2.2	HECS Schematic	4	8-Sep-07	11-Sep-07
2.2.3	HECS PCB Layout	2	8-Sep-07	9-Sep-07
2.2.4	HECS Packaging	3	11-Sep-07	13-Sep-07
2.3.1.1	Program Architecture	4	8-Sep-07	11-Sep-07
2.3.1.2	Software Initialization	2	11-Sep-07	13-Sep-07
2.3.1.3	Program Tasks Management	4	13-Sep-07	16-Sep-07
2.3.2.1	Plugin Software Architecture	4	7-Oct-07	10-Oct-07
2.3.2.2	Plugin Initialization and Negotiation	4	7-Oct-07	10-Oct-07
2.3.2.3	Plugin Communications Protocols	3	10-Oct-07	12-Oct-07
2.3.3.1	uC Program Architecture	2	15-Sep-07	16-Sep-07
2.3.3.2	uC Data Transfer	4	12-Sep-07	15-Sep-07

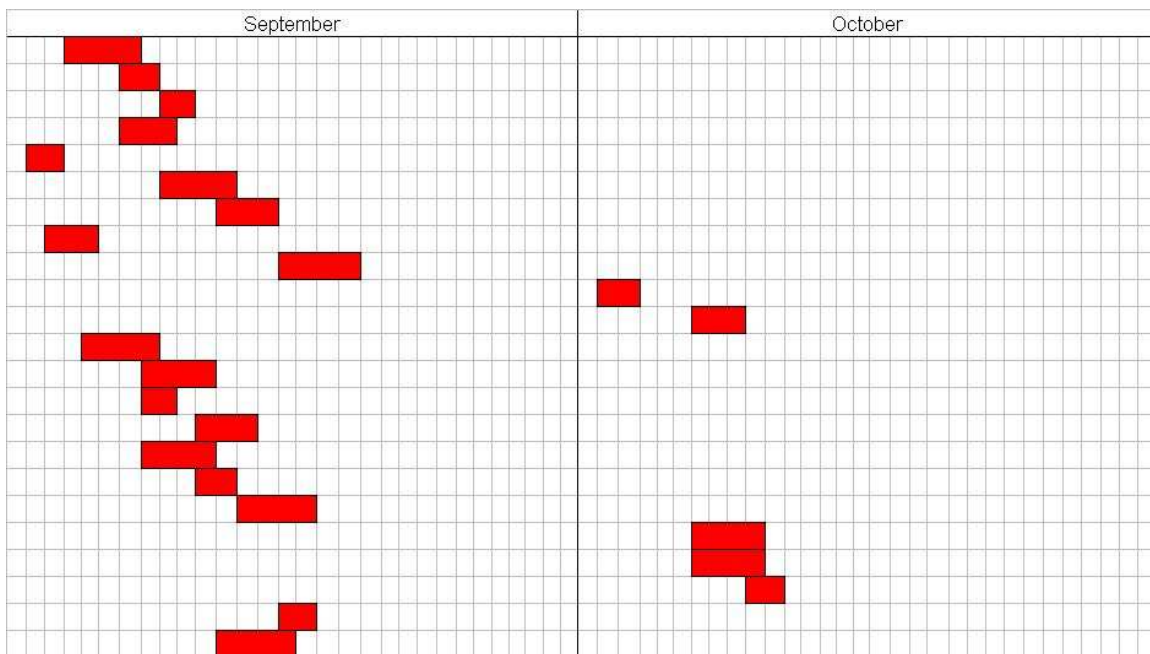
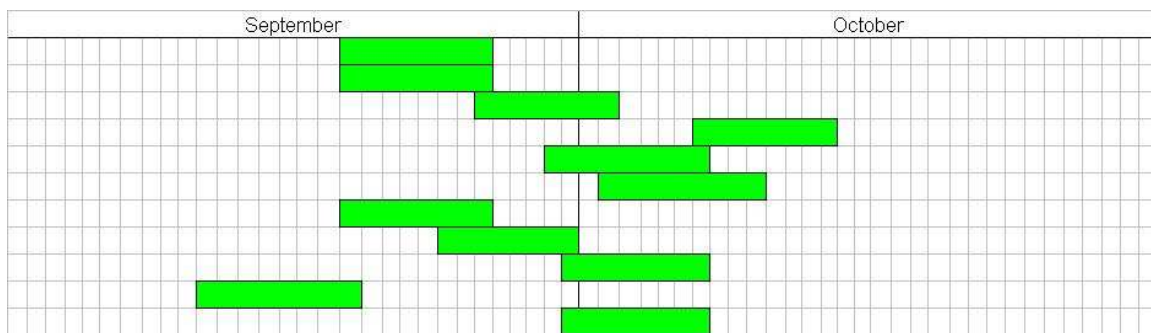


Figure 4. Design Phase Gantt Chart.

**Table 3. Procurement Phase Gantt Tasks.**

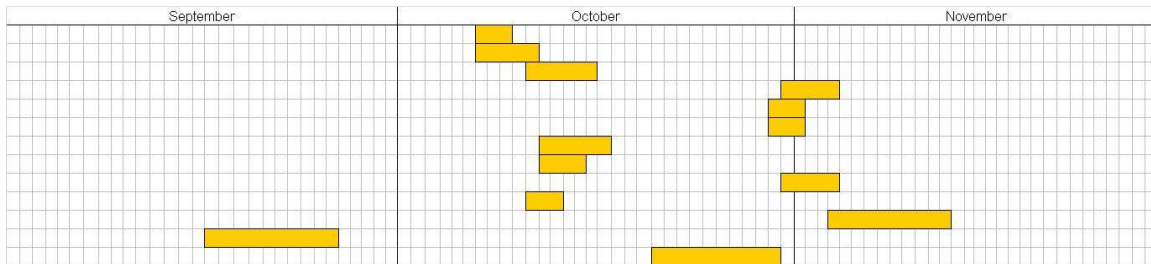
Procurement Phase				
3.1.1	BPL Chipset	8	18-Sep-07	25-Sep-07
3.1.2	Microcontroller	8	18-Sep-07	25-Sep-07
3.1.3	Power Supply	8	25-Sep-07	2-Oct-07
3.1.4	PCB Board	8	7-Oct-07	1014/2007
3.1.5	Flashable Boot Memory	8	29-Sep-07	6-Oct-07
3.1.6	Miscellaneous small components	8	2-Oct-07	7-Oct-07
3.2.1	IR Transmitter	8	18-Sep-07	25-Sep-07
3.2.2	IR Driver	8	23-Sep-07	30-Sep-07
3.2.3	Flashable Memory	8	30-Sep-07	7-Oct-07
3.2.4	PCB Board	8	11-Sep-07	18-Sep-07
3.2.5	Miscellaneous small components	8	30-Sep-07	7-Oct-07



**Figure 5. Procurement Phase Gantt Chart.**

**Table 4. Implementation Phase Gantt Tasks.**

Implementation Phase				
4.1.1.1	BPL Power	3	7-Oct-07	9-Oct-07
4.1.1.2	BPL Data Signaling	5	7-Oct-07	11-Oct-07
4.1.2	Microcontroller	6	11-Oct-07	16-Oct-07
4.1.3	Power Supply	5	31-Oct-07	4-Nov-07
4.1.4	Flashable Boot Memory	3	29-Oct-07	31-Oct-07
4.1.5	Volatile Memory	3	29-Oct-07	31-Oct-07
4.2.1	IR Transmission	6	12-Oct-07	17-Oct-07
4.2.2	IR Codes in flash memory	4	12-Oct-07	15-Oct-07
4.3.1.1.1	uC Data Processing	5	31-Oct-07	4-Nov-07
4.3.1.1.2	BPL Communication	3	11-Oct-07	13-Sep-07
4.3.1.1.3	Write uC Code	10	4-Nov-07	13-Nov-07
4.3.1.2	Write WireNet GUI	10	16-Sep-07	25-Sep-07
4.3.2	Write HECS GUI	10	21-Oct-07	30-Oct-07



**Figure 6. Implementation Phase Gantt Chart.**

Table 5. Testing Phase Gantt Tasks.

Testing Phase				
5.1.1.1	Test uC Hardware	5	4-Nov-07	8-Nov-07
5.1.1.2	Test uC Code	5	4-Nov-07	8-Nov-07
5.1.2	Test Results	2	8-Nov-07	10-Nov-07
5.2.1.1	Test Communication with uC	5	4-Nov-07	8-Nov-07
5.2.1.2	Test Communication over Powerline	3	8-Nov-07	10-Nov-07
5.2.2	Test Results	3	10-Nov-07	12-Nov-07
5.3.1.1	Test WireNet Interface	5	25-Sep-07	29-Sep-07
5.3.1.2	Test BPL Chipset	5	4-Nov-07	8-Nov-07
5.3.1.3	Test Power Supply	4	4-Nov-07	7-Nov-07
5.3.2	Test Results	3	8-Nov-07	10-Nov-07
5.4.1.1	Test HECS Interface	4	30-Oct-07	2-Nov-07
5.4.1.2	Test IR Transmission	5	17-Oct-07	21-Oct-07
5.4.1.3	Test Flash Memory	2	30-Oct-07	31-Oct-07
5.4.2	Test Results	3	2-Nov-07	4-Nov-07
5.5.1.1	Test BPL Communication	5	10-Nov-07	14-Nov-07
5.5.1.2	Test Software Communication with uC	5	10-Nov-07	14-Nov-07
5.5.1.3	Test User Interface	5	10-Nov-07	14-Nov-07
5.5.2	Test Results	3	14-Nov-07	16-Nov-07

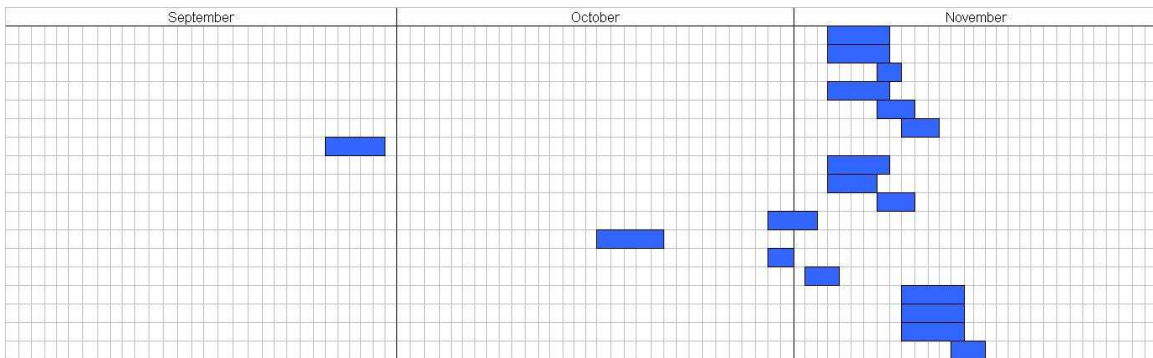


Figure 7. Implementation Phase Gantt Chart.



Table 6. Documentation Phase Gantt Tasks.

Documentation Phase				
6.1.1	Circuit Schematic	3	12-Nov-07	14-Nov-07
6.2	Parts List	2	16-Nov-07	17-Nov-07
6.3.1	Installation Guide - WireNet & HECS Installation	3	16-Nov-07	18-Nov-07
6.3.2	Installation Guide - Verification of Operation	3	16-Nov-07	18-Nov-07
6.3.3	Installation Guide - Troubleshooting	3	16-Nov-07	18-Nov-07
6.4.1	User's Manual - Specifications	3	16-Nov-07	18-Nov-07
6.4.2	User's Manual - Schematics	3	16-Nov-07	18-Nov-07
6.4.3	User's Manual - Operation	2	18-Nov-07	19-Nov-07
6.4.4	User's Manual - FAQ	2	18-Nov-07	19-Nov-07
6.4.5	User's Manual - Troubleshooting	2	18-Nov-07	19-Nov-07
6.4.6	User's Manual - Safety Precautions	1	18-Nov-07	18-Nov-07
6.5.1	Flowcharts	2	12-Nov-07	13-Nov-07
6.5.2	Pseudo Code	2	12-Nov-07	13-Nov-07
6.5.3	Hierarchy Charts	2	12-Nov-07	13-Nov-07
6.6	Demonstration of Operation	1	19-Nov-07	19-Nov-07

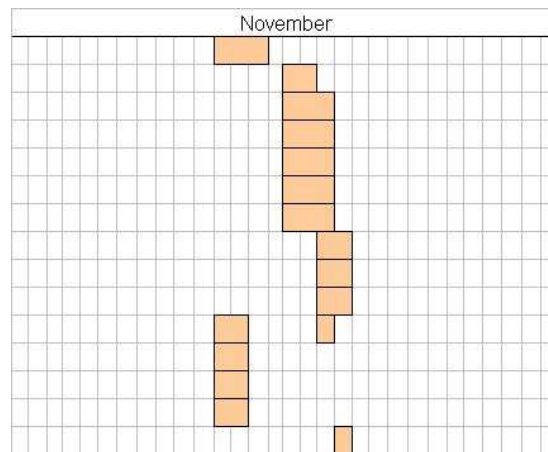


Figure 8. Documentation Phase Gantt Chart.