SONY

Chapter 3 Semiconductor Device Failure Analysis

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Semiconductor Quality and Reliability Handbook

Chapter 3 Semiconductor Device Failure Analysis

3.1 What is Failure Analysis?

Failure analysis consists of swiftly confirming various failure conditions that occur in the various manufacturing processes and the market, investigating the electrical characteristics using a LSI tester and other tools, and then using these results together with the optimum physical and chemical methods and analysis equipment to clarify the causes and mechanisms that led to the failures.

3.2 Necessity of Failure Analysis Technology

Chips used in semiconductor devices are becoming more highly integrated and products are incorporating more advanced functions in recent years, such as multiple chips mounted in a single package (SIP: System in Package). As a result, manufacturing processes are becoming more miniaturized and complex, and failure causes and mechanisms are also diversifying and becoming more complex.

However, extremely high levels of quality and reliability are required of semiconductor devices. When manufacturing semiconductors, consistent quality and reliability must be built in from the development stage to the manufacturing stage in order to prevent semiconductor devices from failing in the market and causing trouble for customers. For this reason, it is extremely important to swiftly analyze failed products occurring in reliability tests, customer processes and the market, accurately clarify failure causes and mechanisms, and provide feedback to the manufacturing and design processes to improve manufacturing and product quality.

In this manner, failure analysis technology is not simply a means to investigate the failure causes and mechanisms of failed products. It is a vital and essential technology for quality and reliability improvement activities aimed at reducing failures in customer processes and the market to as close to zero as possible.

3.3 Failure Analysis Technology

3.3.1 General Failure Analysis Flow

The most important factor in failure analysis is how far the failure location can be narrowed down while still maintaining the failure symptoms (undestroyed state). The failure cause clarification rate varies widely according to whether the location can be narrowed down only to the function block level or whether the location of the trouble can be pinpointed.

Finding a failure location with a radius of approximately 1 μm in the latest highly integrated semiconductor devices is comparable to searching for a coin dropped somewhere in an eight-story building covering a site the size of a baseball stadium. In this type of situation it is impossible to find the location simply by searching with only a vague notion of where to look.

The chances of finding the coin can be increased by first carefully investigating the behavior and other details of the person who dropped the coin, isolating as much as possible the location where the coin is thought to have been dropped, and then searching carefully once that location has been determined.

Likewise, isolation of a semiconductor device failure location begins by investigating the electrical characteristics with an LSI tester and other tools in order to roughly narrow down the part of the device where the failure is likely to have occurred.

Fig. 3-1 shows an example of general failure analysis procedure.

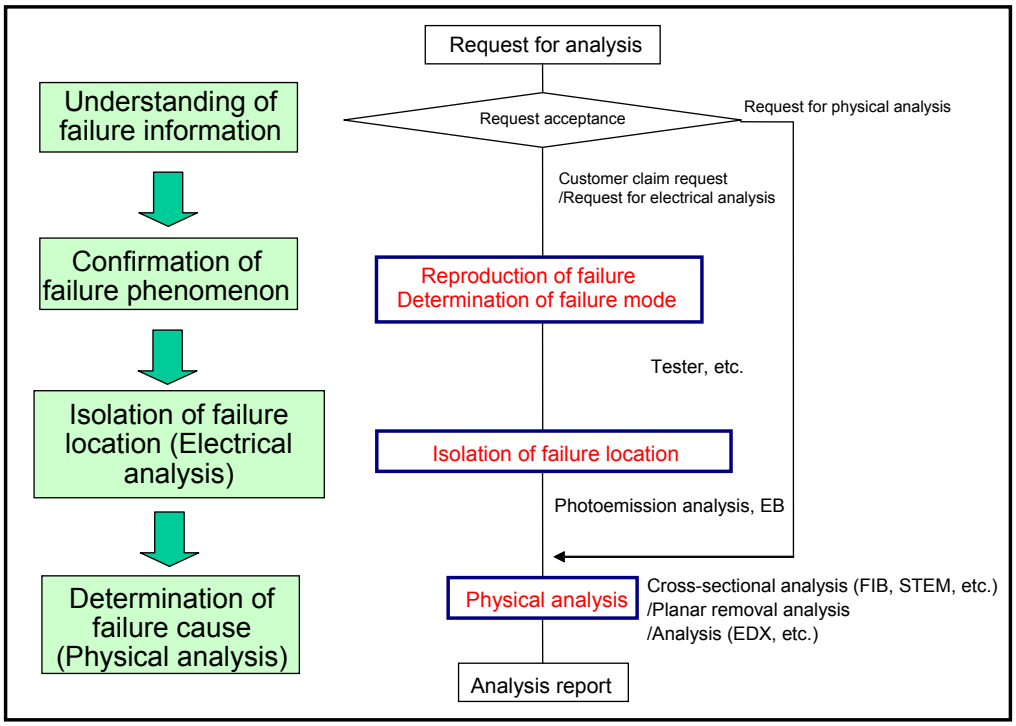


Fig. 3-1 General Failure Analysis Procedure

Each item is described in detail in the following sections.

3.3.2 Investigation of Failure Circumstances

When failures occur, the failure circumstances (whether the failure occurred in the customer's manufacturing process or after the product had been used in the market for a while, what was the operating environment, etc.) are extremely important information for estimating the failure cause and determining the failure analysis methods and procedures so that failure analysis can proceed smoothly.

Therefore, when a failure sample is obtained, as much information as possible about that sample is gathered at the same time from the customer and other sources. Information about the environment in which the failure occurred (place where the trouble occurred, environmental conditions, circuits used, operating conditions, mounting conditions, etc.) is particularly helpful in estimation of the failure mechanism and selection of analysis techniques and methods. In addition, such information is sometimes helpful in performing failure simulations and confirming reproducibility in order to help determine whether the failure is a random failure or due to a design problem.

3.3.3 Handling of Failure Samples

Failure samples are highly valuable as their number is limited. If failure analysis is unsuccessful, it is possible that no information may be obtained. Therefore, the following precautions should be observed when handling failure samples.

(1) Maintenance of failure conditions

If stress (thermal, electrical, mechanical) that may change the failure conditions is applied prior to analysis, analysis is impossible. However, if samples are removed from boards after being solder-mounted onto boards, lead processing or reball operation is required for LSI tester measurement.

The utmost care should be taken during these heating processes to conduct them in as short a time as possible and not to apply heat to the device or to damage the leads or lands. The Sony Semiconductor Business Unit has also prepared an environment that enables electrical measurement in the land grid array (LGA) state (the same state as when the solder balls are removed from a BGA product) as a method of analyzing ball grid array (BGA) products without applying heat.

(2) Storage

Care must be taken to store failure samples in an environment with the ideal temperature and humidity, and to prevent electrical, mechanical and other damage.

Additional care must also be taken for storage to prevent the adherence of dust or surface scratching of samples with decapped packages or that have been reduced to discrete chips partway through physical analysis. Recently it has also become necessary to store samples in locked storage vaults or rooms that ensure a certain level of security to prevent information leaks concerning security chips and other confidential technology.

3.3.4 External Visual Inspection of the Package

Visual inspection of the external condition of the obtained samples is extremely important, and is a source of useful information for failure analysis. The main check contents are cracking, voids, scratching, burn marks, damage to external pins, adherence of foreign matter, discoloration, etc.

3.3.5 Evaluation of Electrical Characteristics

(1) Evaluation using an LSI tester

First, the electrical characteristics of failure samples are evaluated by test programs similar to those used for the shipping inspection. These results are then used to determine whether the product failed due to a semiconductor defect, or whether a product that should normally have failed the shipping inspection inadvertently flowed out to a customer due to some deficiency with the test program. In addition, the temperature dependence, voltage dependence, operating frequency dependence and other details of the failed product are evaluated, and the obtained data is used to determine the detailed analysis methods.

(2) AC and DC characteristics evaluation

Open connections, short circuits, withstand voltage deterioration and other DC characteristics are investigated using a curve tracer, parameter analyzer and other tools. In addition, an oscilloscope is used for simple AC characteristics evaluation, etc.

(3) Evaluation using actual electronic equipment (evaluation jig created by modifying an actual set product)

When the failure cannot be reproduced by the checks described above and the failure sample receives a passing judgment (the product passes the assurance items for a discrete semiconductor device), failure reproducibility is checked using an evaluation jig created by modifying an actual set product, etc.

If the trouble is confirmed at this point, the function trouble occurring in the actual set product may be a case not included in the shipping inspection program using the LSI tester, so addition to the function test items is investigated. This method is also used as a means of analysis (in place of an LSI tester, etc.) to narrow down the failure location when the failure is reproduced but the location is difficult to narrow down using methods (1) and (2) above.

3.3.6 Package Analysis Technology

3.3.6.1 Description

Recently, compact semiconductor products with advanced functions that incorporate peripheral devices into a thin package are demanded. These needs are met by SiP products, which have recently become the main product type. Fig. 3-2 shows a schematic of a typical SiP product. Package on Package (POP) products have also appeared, in which multiple chips are stacked in a single package and not only chips but actual products are incorporated. As a result, structures are becoming extremely complex, making it necessary to clarify whether the failure occurred inside a chip or if it is rooted in the assembly before starting detailed analysis. In addition, increasing numbers of pins and other factors are resulting in extremely narrow metal wiring intervals, and even microscopic foreign matter that previously was not a problem can cause short-circuits between wiring, so material control and assembly process cleanliness requirements have also become extremely strict compared to previous levels. This also applies to decapping methods. For example, decapping that uses only fuming nitric acid or other chemicals is insufficient to analyze diverse structures, so new decapping methods must also be investigated.

In this section, conventional package analysis methods are simply described, and new equipment and methods being actively introduced by the Sony Semiconductor Business Unit to analyze the latest package structure products are mainly focused on.

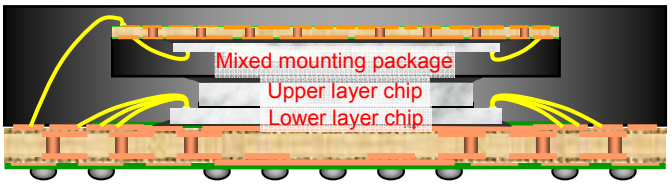


Fig. 3-2 Schematic of Typical SiP Product

3.3.6.2 X-ray Observation and Scanning Acoustic Tomography Observation

X-ray observation allows non-destructive observation of the wire bonding condition (wire loop condition, gold bump condition, switch shape, etc.), lead frame condition, voids in the molded resin, and the board wiring and through-hole condition. In addition, recent improvements in radiograph resolution also enable observation of the condition of micro-bumps used in Chip on Chip (CoC) and other packages. (See Fig. 3-3.)

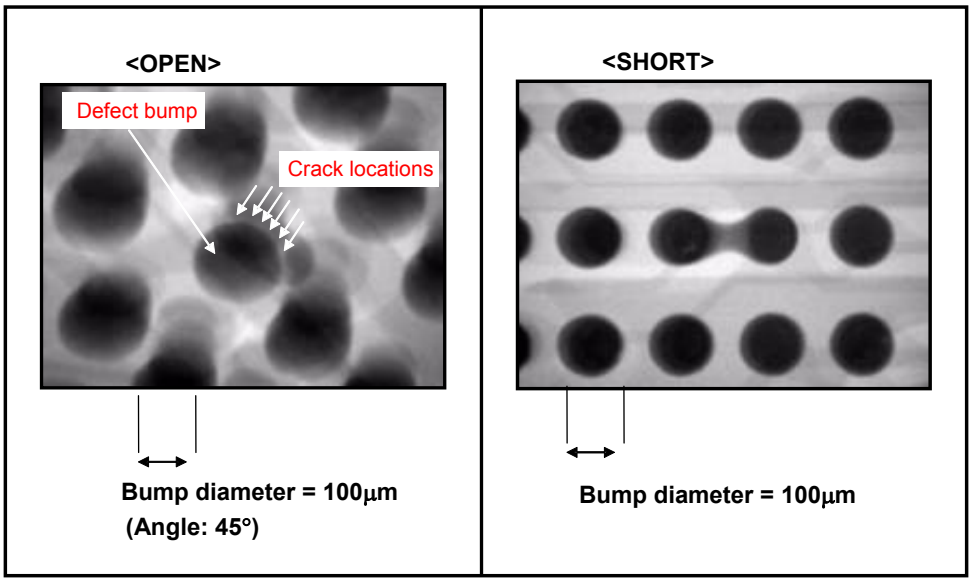


Fig. 3-3 X-ray Photo

The addition of CT functions has also enabled three-dimensional confirmation of internal structures in the undestroyed state, making radiographs useful equipment for observing assembly trouble.

Scanning acoustic tomographs (SAT) and scanning acoustic microscopes (SAM) use the principle that ultrasonic waves are reflected at the junction interface between materials with different acoustic impedance. SAT and SAM detect the reflected waves of the ultrasonic waves emitted to the sample, enabling non-destructive observation of package internal conditions at arbitrary depths, such as junction interface delamination, voids in the package resin, cracks, and chip cracking. (See Fig 3-4.)

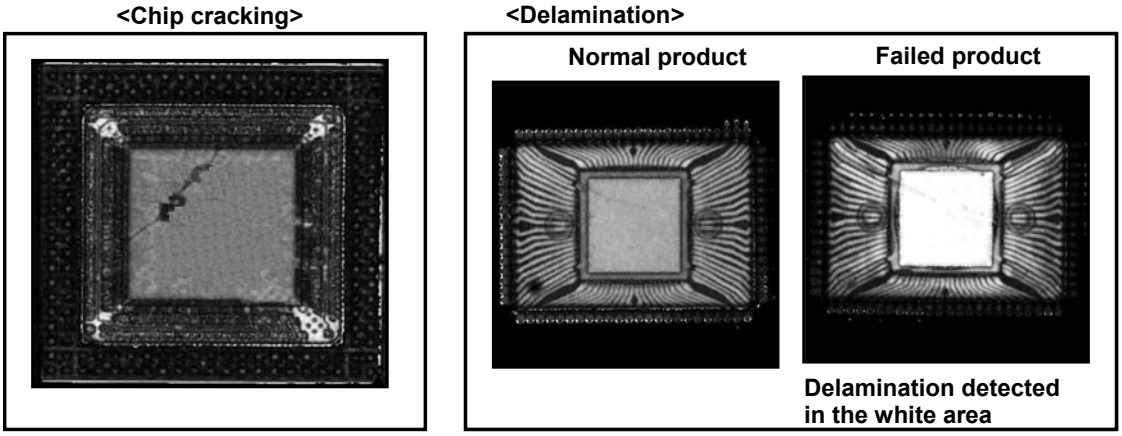


Fig. 3-4 Scanning Acoustic Tomography Photo

Recently, higher frequencies (approximately 300 MHz) are used to increase the resolution, enabling observation of interface delamination like micro-bumps as small as approximately 40 μm and internal voids.

The equipment outline and principle are typical and have been described in various documents, so these descriptions are omitted here.

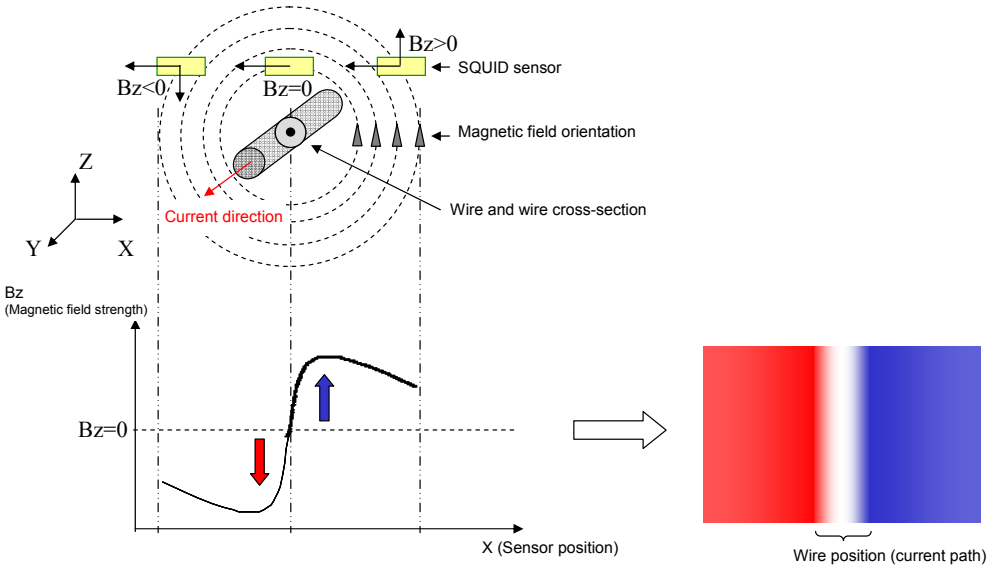
3.3.6.3 New Technologies that have Begun to be Used in Recent Years

(1) Scanning SQUID (Superconducting QUantum Interference Device) Microscope Analysis

SQUID is the abbreviation for an ultra-sensitive magnetic sensor that uses the superconducting quantization phenomenon. SQUID has far greater sensitivity than conventional magnetic sensors, and can detect weak magnetic fields on the order of 1/50,000,000 of terrestrial magnetism or less.

It is known that a magnetic field is generated around flowing current. (See Fig. 3-5.) As described above, SQUID uses an ultra-sensitive magnetic sensor, so it can detect the magnetic fields generated by currents.

The currents flowing inside a semiconductor device can be observed by using the obtained magnetic field distribution information to create images of the currents that generate that magnetic field distribution. (See Fig. 3-6.)



Detection of magnetic field strength from a wire

Magnetic field strength vector Bz and wire position

The SQUID sensor acquires the magnetic field strength and plots it on a graph.
The magnetic field strength is zero in the Z direction directly above the wire.

Graphical representation of magnetic field

The magnetic field strength Bz is simulated using color. Blue is displayed when magnetic field strength Bz > 0, and red when Bz < 0.
In addition, the magnetic field strength is expressed by the color density. The area directly above the wire is displayed as white, indicating that this is the current path.

Fig. 3-5 Scanning SQUID - Graphical Representation of Current and Magnetic Field

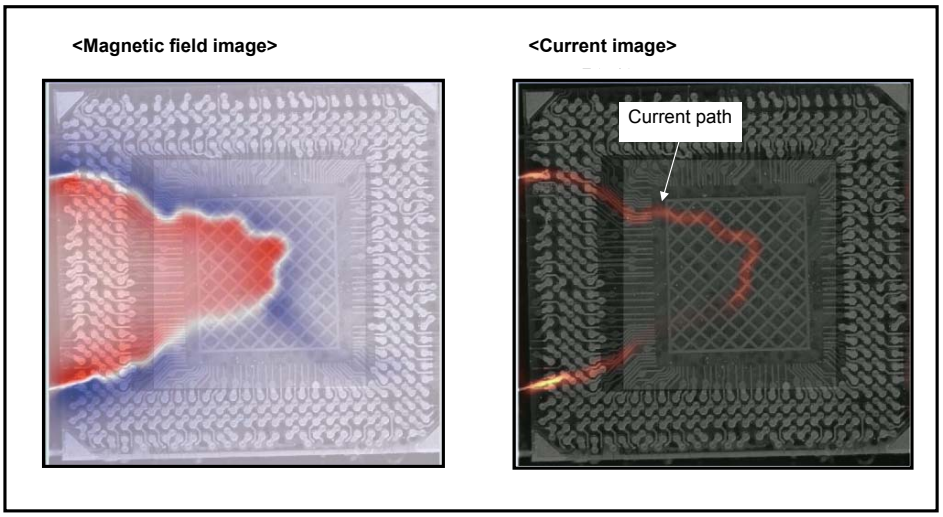


Fig. 3-6 Scanning SQUID - Magnetic Field and Current Images

In addition, magnetism passes through silicon and most other materials used in semiconductor devices and packages, so current paths can be observed in a non-destructive manner, which is a merit for failure analysis. However, given the nature of the principle that current paths are shown by detecting magnetic fields, failure analysis using this equipment is valid only in the DC measurement state where the current direction is constant. Actual failure analysis is performed by first comparing the observed current paths of good and failed products to narrow down the location of the failure cause, and then performing detailed analysis to clarify the cause.

An example of analysis using this method is shown below. (See Fig. 3-7.)

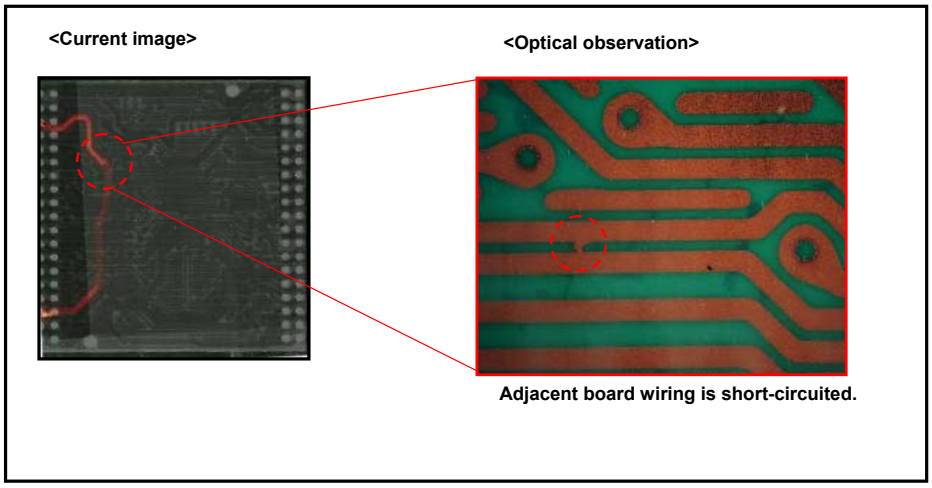


Fig. 3-7 Example of Using Scanning SQUID to Determine Foreign Matter

These results show that SQUID can also determine failure causes due to microscopic conductive foreign matter that would be difficult to discover by X-ray observation.

(2) TDR (Time Domain Reflectometry) Analysis

TDR is a technique that measures the transfer quality of a measured item by inputting a high-speed pulse signal to the measured item and observing the reflected signal. This method has a long history of use to discover broken power transmission lines and other failures. (See Fig 3-8.)

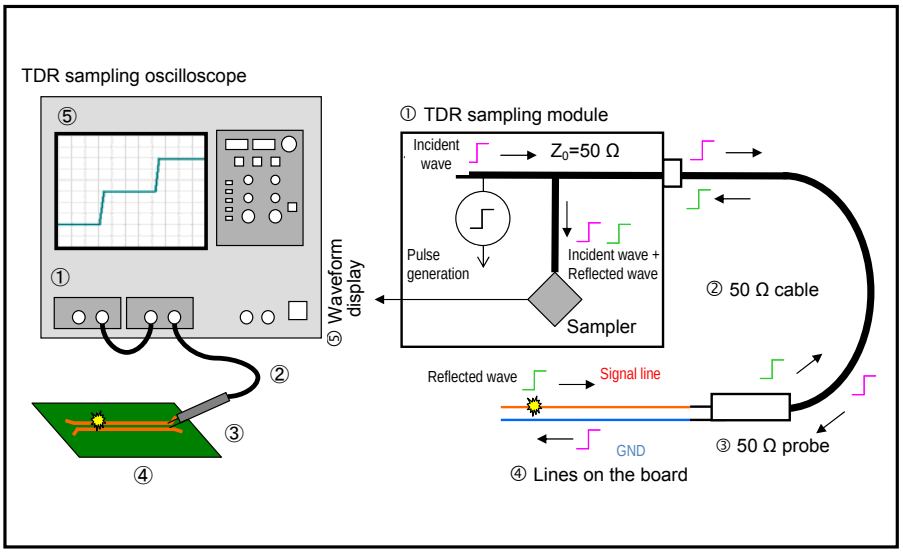


Fig. 3-8 General Principle of TDR

This technique is applied to semiconductor package analysis. Here, a probe is connected to the package electrode linked to the presumed trouble location, a high-speed pulse signal is applied to the sample, and a sampling oscilloscope is used to observe the reflected waves generated at locations with material impedance mismatch. When the wiring line contains an open wiring connection or other open defect, the impedance mismatch increases at the trouble location, generating a large reflected wave that appears as a difference between the good product and failed product waveforms. The failure location can be inferred from this reflected wave difference. This principle can also be applied to determine short-circuit locations, but currently it is mainly used to determine open locations.

Like the previously described SQUID analysis, TDR also enables non-destructive analysis, and especially as there are no other methods at present that can swiftly determine open locations in a non-destructive manner, it is an extremely useful analysis method for analyzing semiconductor device packages. In particular, the boards used in SiP and other advanced function products are arranged in multiple layers, so overlapping wiring and other influences make it difficult to determine trouble simply using X-ray observation. Therefore, failure locations are first reliably narrowed down using TDR, and then X-ray observation and other analysis methods are performed.

An example of analysis using this technique is shown below. (See Fig. 3-9.)

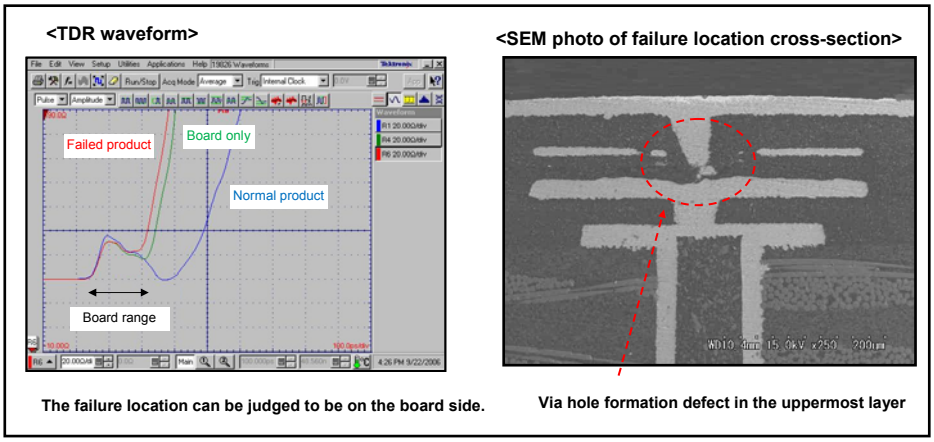


Fig. 3-9 Example of Failure Determination Using TDR

(3) Cross-section machining by a cross-section polisher (CP)

When observing a cross-section in assembly-related failure analysis, the subject observation range is wide in many cases, so mechanical polishing was mainly used. However, mechanical polishing uses sandpaper and abrasives, so there are limits to the finish of the machined surface, and in particular the solder, gold, copper, aluminum and other materials often used in assembly are soft, which produces sagging on the surface. This made it difficult for unskilled workers to realize a completely mirror finish, and led to problems such as the inability to see microscopic cracking depending on the finishing method.

In addition, a mirror finish can easily be obtained by using a focused ion beam (FIB) such as that used in chip cross-sectional analysis, etc. However, FIB is normally used to machine microscopic areas (on the level of several μm), so there are various issues compared to mechanical polishing, such as 1) machining takes an extremely long time, and 2) unsuitability for machining wide areas.

CP cross-section machining combines the convenience and swiftness of mechanical polishing with the ease of obtaining a surface mirror finish of FIB machining.

A cross-section polisher (CP) can create a relatively damage-free cross-section by aligning the location to be machined with a shielding plate and irradiating an Ar ion beam. Use of this equipment enables easy and reliable observation of interface conditions where multiple materials are joined, such as for example the bonding interface between gold wire and an aluminum pad, and microscopic voids and cracking. (See Fig. 3-10 and Fig. 3-11.)

<Solder Bump>

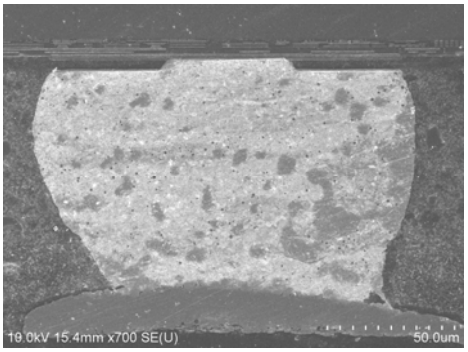


Fig. 3-10 Observation Photo after Mechanical Polishing

<Solder Bump>

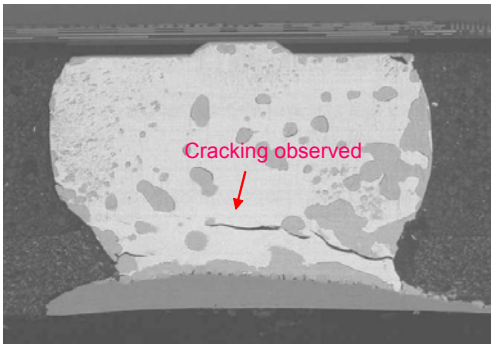


Fig. 3-11 Observation Photo after CP

3.3.7 Chip Analysis Technology

3.3.7.1 Description

As previously mentioned, products are becoming more highly integrated and incorporating more functions in recent years. As a result, circuits are also increasing vastly in both scale (several ten to hundred million gates) and complexity, which means that it is not an easy task to narrow down the locations of failures on a level of several μm and clarify the causes. A variety of methods are used to narrow down chip failure locations. In addition to photoemission analysis, thermal emission analysis, and IR-OBIRCH (Infra Red-Optical Beam Inducted Resistance CHange), which have traditionally been used to analyze chip failures, software-based failure inference technology and other methods have also appeared.

In addition, new analysis methods such as dynamic laser stimulation (DLS) analysis and micro probing technology have also appeared recently, and the current situation is that multiple analysis methods are combined to narrow down failure locations that previously could not be determined. This has also greatly increased the time required for failure analysis. Therefore, in addition to improving the failure cause determination rate, shortening the turn-around time (TAT) from analysis start to finish has also come to be an issue for current failure analysis technology.

The roles, functions and other features of the main analysis methods used to determine failure locations in various chips are described below.

3.3.7.2 Package Decapping Technology and Stacked Chip Removal Technology

There are various package types such as packages that use mold resin and packages that use ceramics. This section describes decapping of mold resin, which is the type most commonly used. The basic decapping method consists of using chemicals to dissolve the resin and expose the chip surface.

Decapping methods include the following:

1) Automatically using an acid decapsulator

2) Manually by workers using tools

It is generally recognized that when 1) using an acid decapsulator, decapping skill and experience are not required, and packages can be decapped easily even by unskilled workers. However, there are various issues such as that work conditions during decapping cannot be viewed from the outside so the decapping progress cannot be known, and the etching rate varies easily due to even small shifts in the chemical solution temperature, flow rate and other conditions. Therefore, this method is not very suitable for decapping when the electrical characteristics are to be maintained.

When analyzing a complaint with a small number of samples, if a mistake is made during the decapping work, further analysis can become next to impossible, so the Sony Semiconductor Business Unit performs decapping manually in most cases. Recently, resins that cannot be decapped using chemicals are increasing, so efforts are underway to find alternate methods. However, the ideal methods have yet to be found, and the establishment of technology in this field is an urgent issue.

In addition, SiP and other products are assembled by stacking multiple chips. In these cases, when the chip subject to failure analysis is located in a lower level, the chips and other items stacked in the upper levels hinder analysis and must be removed. However, it is essential to avoid damaging the sample subject to failure analysis when removing upper-layer chips. To achieve this, the Sony Semiconductor Business Unit has established technology that reliably removes unnecessary stacked chips and other items without mistakes by using milling machines that enable highly accurate machining control. (See Fig. 3-12.)

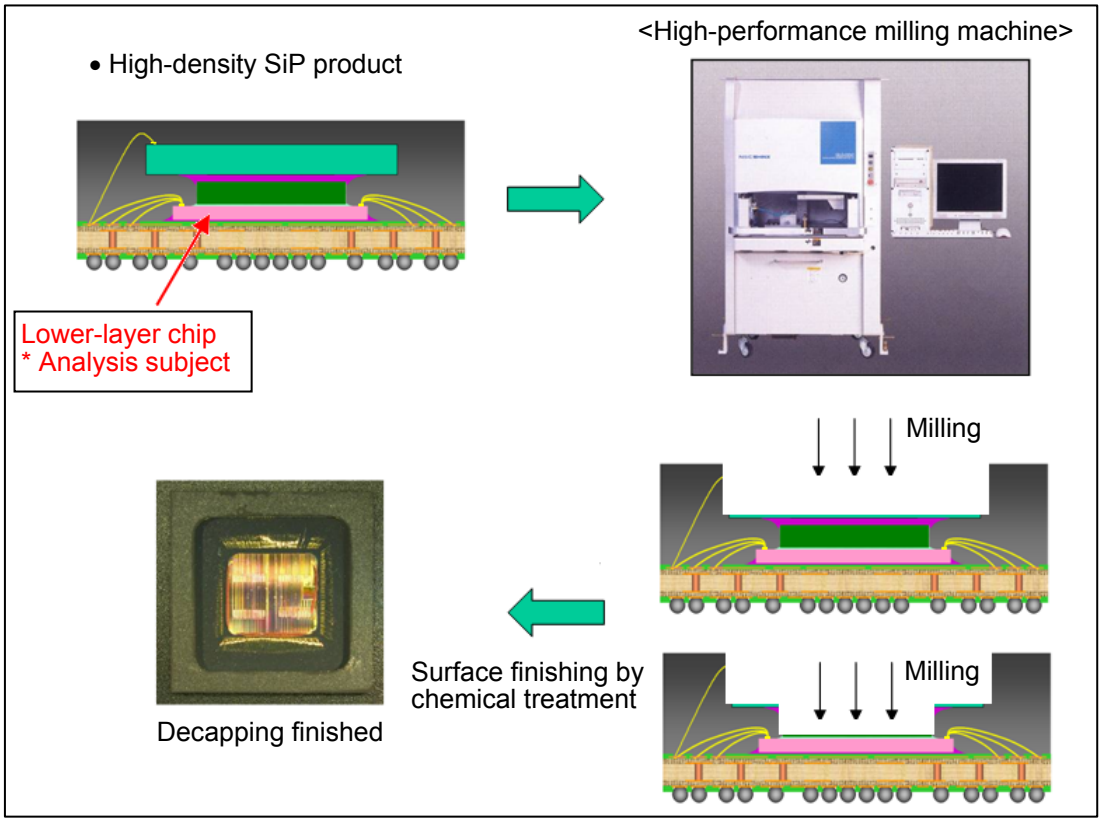


Fig. 3-12 High-Performance Milling Technology

3.3.7.3 Failure Locating Technology

Mechanical probing, electron beam (EB) testing, photoemission analysis, thermal emission analysis and other technologies are widely known as conventional technologies for determining failure locations inside chips. Semiconductor devices are becoming more miniaturized, highly integrated, multi-functional, and higher speed in recent years, with the result that cases where failures cannot be found by using only one of these analysis methods are increasing. This is making it necessary to use multiple analysis methods including even newer methods to narrow down and pinpoint failure locations. However, the combination of methods used to narrow down the location must be determined each time from information obtained when checking the electrical characteristics, so it is difficult to provide a specific written rule.

Methods often used for failure analysis and the latest technologies are described below, focusing on the applications and information that can be obtained by each technology when used alone.

3.3.7.3.1 Failure Inference Technology

Recent increases in LSI circuit scales and speeds are greatly increasing the difficulty of circuit electrical analysis. This is because most parts of LSI are configured by complex digital logic circuits, and it has become impossible to narrow down logic circuit failure locations without some clues.

This section describes failure diagnosis technology developed to address this issue. As the name implies, failure diagnosis technology is technology used to diagnose failures, and logic circuit locations experiencing problems can be inferred by using a failure diagnosis test environment created beforehand in the design stage. This failure diagnosis test environment includes a database in which all failures (open wiring connections, short-circuits, etc.) that may possibly occur in the logic circuits are registered. This is called the failure database. In addition, test programs that inspect for failures based on this database are also created, and open wiring connections, short-circuits and other failures that may hypothetically occur in the subject LSI can be detected by running tests using these programs. These test results can also be compared with the failure database to estimate the logic circuit where the failure occurred. These diagnosis results are used as a guide to perform various detailed analyses, which dramatically increases the physical abnormality discovery rate.

Conventional failure diagnosis technology only targeted complete failures such as open wiring connections and short-circuits. However, diagnosis technology that targets signal delay-type failures due to process miniaturization has also recently been developed, and further expansion is expected in the future. (See Fig. 3-13.)

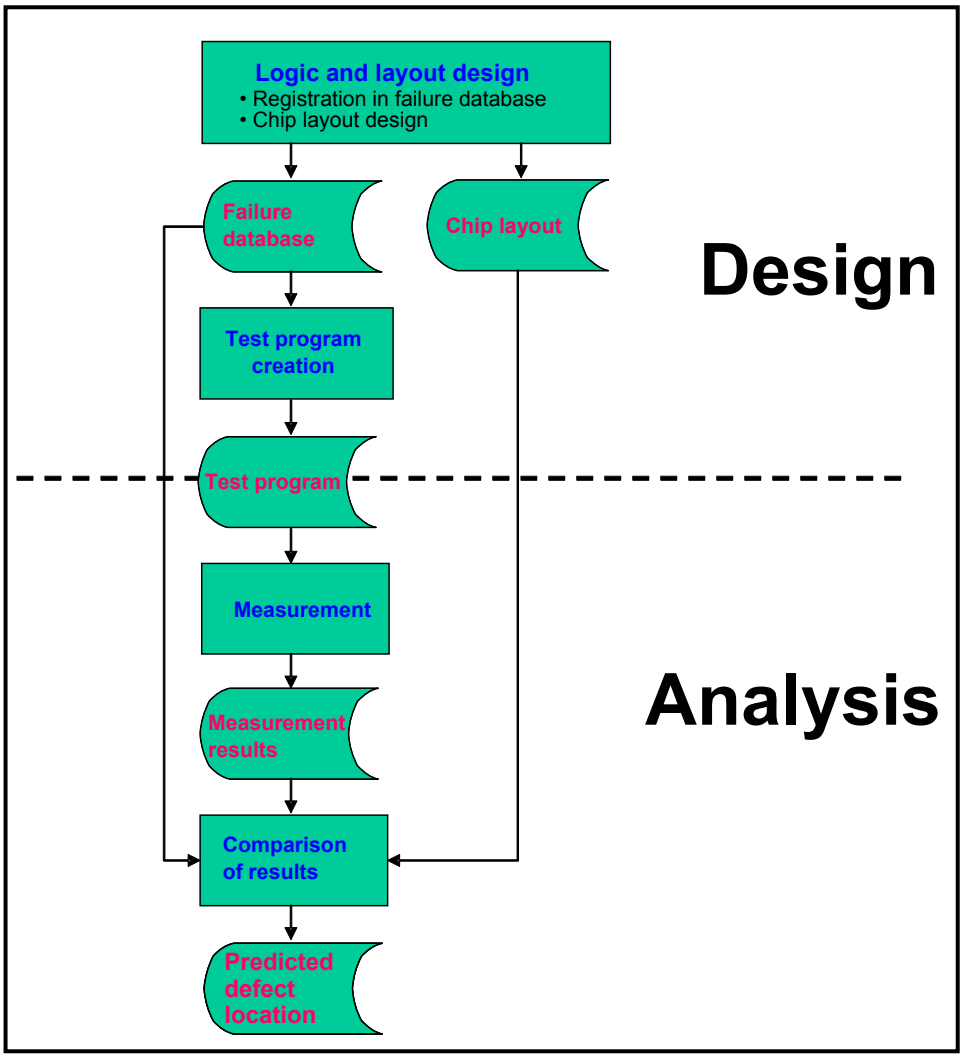


Fig. 3-13 General Failure Inference Flow

3.3.7.3.2 Photoemission Analysis Technology

Photoemission analysis is a well-known method of analyzing current leaks in semiconductor devices.

Current leaks generally involve extremely feeble photoemissions produced by hot electrons and the reuniting of minority carriers.

In addition, through-currents flow due to latch-up and intermediate potential, and current also flows during normal transistor operation, resulting in photoemissions. This method narrows down failure locations by detecting these photoemissions using an ultra-high-sensitivity cooled CCD camera (effective sensitivity approximately 200 nm to 1000 nm) and creating images of the semiconductor device circuit location where the photoemission is occurring. (See Fig. 3-14.)

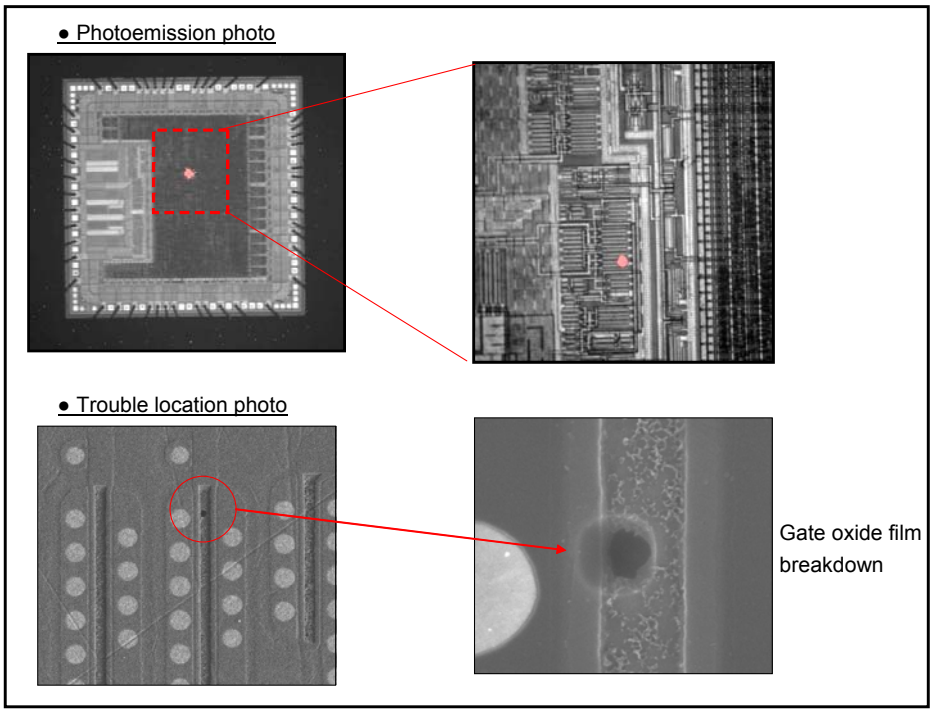


Fig. 3-14 Photoemission Analysis Photos

Recently, MCT cameras that have improved sensitivity in the infrared wavelength range and new-type InGaAs cameras (effective sensitivity approximately 800 nm to 2000 nm) have also appeared. These cameras have extremely good sensitivity characteristics in the infrared range, and are highly effective at capturing photoemissions from the rear surface of the chip. The photoemission analysis method is used to analyze highly integrated semiconductor devices with multilayer wiring by observing infrared light transmitted through the silicon, from the rear surface of the chip.

In addition, InGaAs cameras tend to be incorrectly thought of as having higher sensitivity than general cooled CCD cameras, but the wavelength band captured by each camera type differs, so it cannot be absolutely said that one has higher sensitivity than the other. However, silicon is mainly used as the material surrounding the transistors, so InGaAs cameras with extremely good sensitivity for infrared light that easily passes through silicon are advantageous for analysis of recent semiconductor devices. (See Fig. 3-15.)

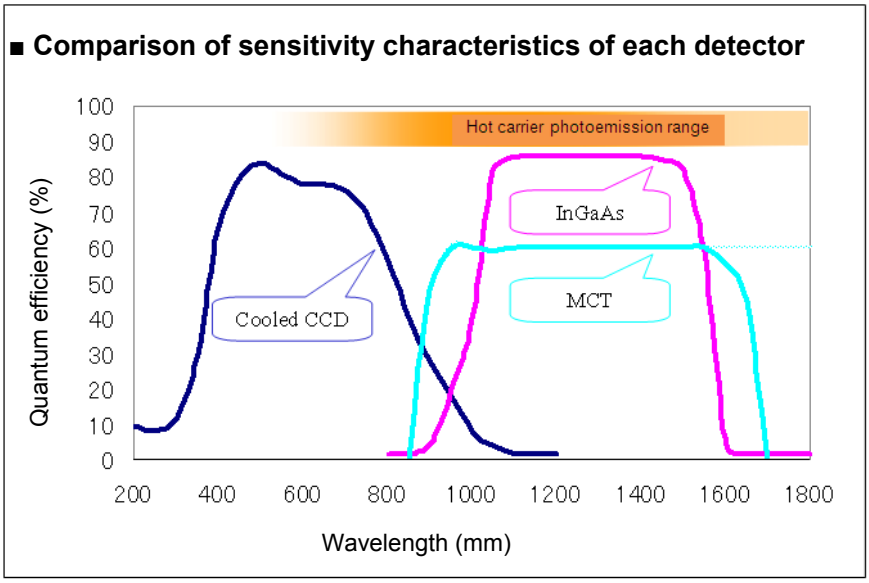


Fig. 3-15 Photoemission Sensitivity Characteristics of Each Detector

One merit of the photoemission analysis method is that analysis can be performed in either the AC or DC state. However, current flow involves some photoemission, so thorough care must be taken to correctly interpret the significance of photoemission captured by photoemission analysis.

All photoemission locations are not necessarily failure locations. Therefore, it is important to not rely only on photoemission analysis, but to combine multiple analysis methods so that comprehensive judgment can be made to narrow down failure locations.

3.3.7.3.3 IR-OBIRCH Analysis Technology

This analysis technology uses the following principle to determine short-circuits between wiring, high-resistance areas, and other failures.

- A near-infrared laser is irradiated to partially heat wiring to which a constant voltage is applied.
- The change in temperature causes the wiring resistance to change, with the result that the current flowing through the wiring also changes.
- Failure locations are identified by using a high-sensitivity amplifier to detect this change in current.

As explained by the above principle, this method detects the current change when a failure location is irradiated by a near-infrared laser. Therefore, unlike the previously described photoemission analysis, almost all responding locations are detected as failure locations. However, analysis can be performed only at the DC level, so this method is unsuitable for trouble modes where the failure cannot be reproduced without using an LSI tester or other tool. The near-infrared laser passes through the silicon substrate, so the rear surface of chips can also easily be analyzed. (See Fig. 3-16.)

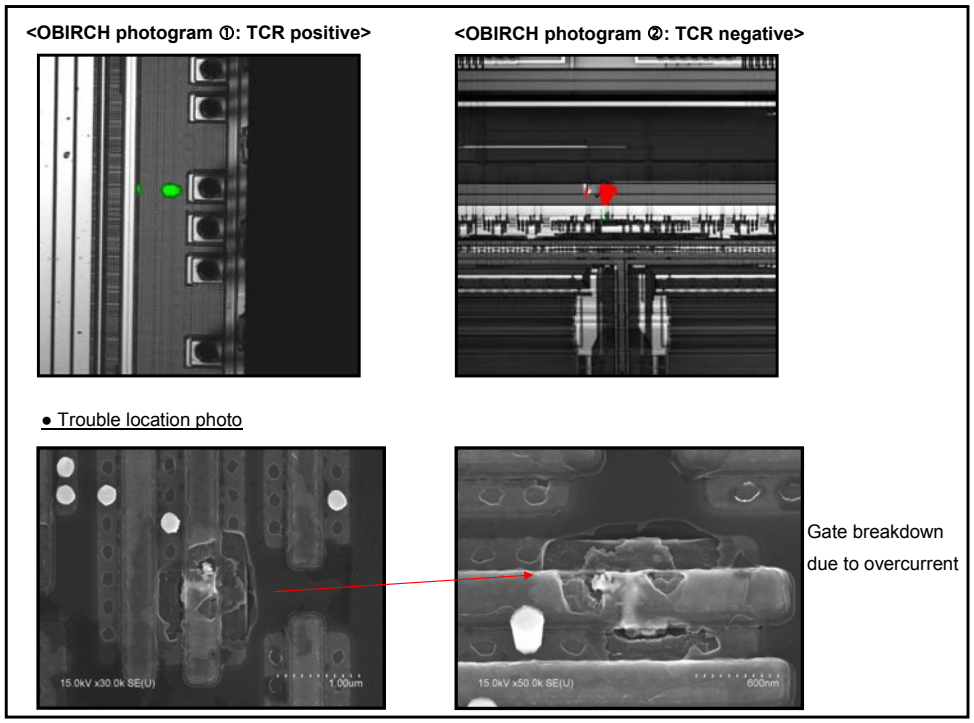


Fig. 3-16 Example of OBIRCH Reaction

3.3.7.3.4 Analysis Technologies that have Begun to be Used in Recent Years

(1) Dynamic laser stimulation (DLS) analysis technology

As semiconductor devices become more miniaturized and faster, marginal failure due to time delays is increasing. Marginal failure is an unstable mode that passes inspection depending on the operating conditions. This makes it difficult to narrow down by existing analysis methods, and recently DLS is gathering attention as an analysis method that can determine this failure.

The DLS analysis method focuses on the fact that most time delay failures are dependent on temperature, and makes use of temperature changes produced by local laser irradiation. When a device is operated using an LSI tester and the device is irradiated from the front or rear surface by an infrared laser with a wavelength of 3.3 μm, the temperature of the irradiated location changes, with the result that the pass/fail status of the device

inverts. This change in the pass/fail status is read from the LSI tester and overlaid with the laser image display to determine the failure location.

DLS is anticipated as an effective analysis method for determining wiring defects such as voids and failures with high temperature dependence such as abnormal transistor characteristics. On the other hand, this analysis method also requires that devices be repeatedly operated for long periods, which makes the condition settings extremely severe, such as temperature control that takes into account the heat generated by the device, and test parameter settings such that the pass/fail status changes when locally irradiated by the laser. (See Fig. 3-17.)

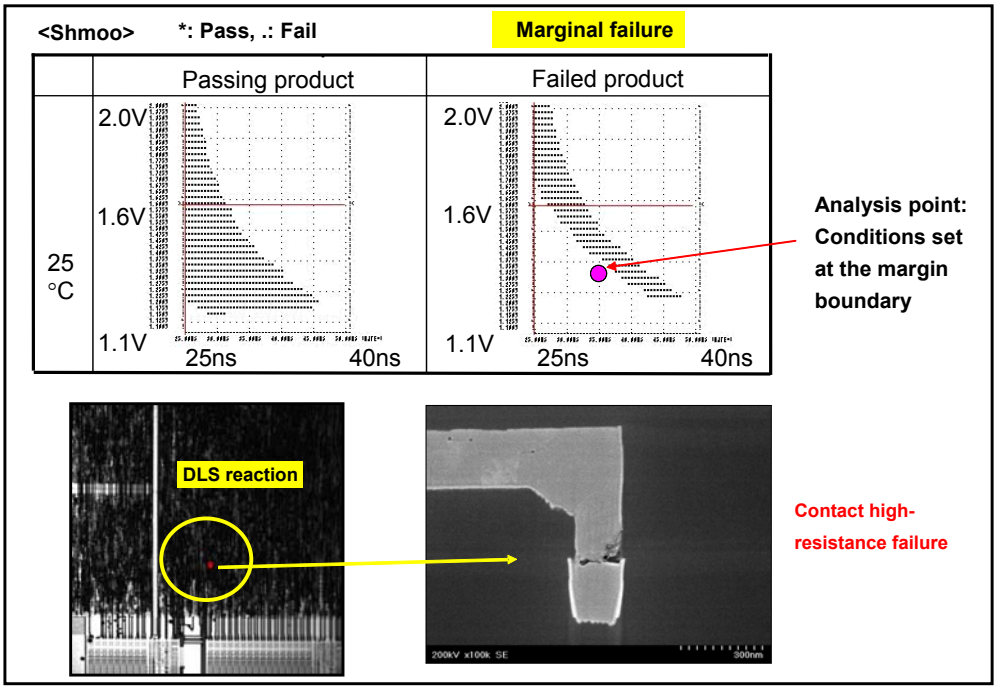


Fig. 3-17 Example of DLS Analysis

(2) Micro probing technology (SEM prober, AMF prober)

This technology obtains the electrical characteristics by directly probing exposed semiconductor element wiring and contacts using a microscopic probe. Mechanical probing using an optical image was formerly the main method, but due to increased miniaturization of semiconductor elements in recent years, the micro probing technologies described below are now the main methods used.

① Probing using an SEM prober

The main probing method is changing from the conventional prober that uses an optical image to a device called a nanoprober that performs probing with a metal probe inserted inside a scanning electron microscope (SEM) while viewing the SEM image. The nanoprober uses a highly accurate probe that can be controlled at the nano level by piezo elements, and a field-emission electron gun that provides high resolution, enabling

direct probing of wiring and contacts in the latest processes. In addition, the nanoprober can also be used together with electron beam absorbed current (EBAC*) technology that uses an electron beam, and is expected to occupy an important position as an analysis method for the latest LSI. (See Fig. 3-18.)

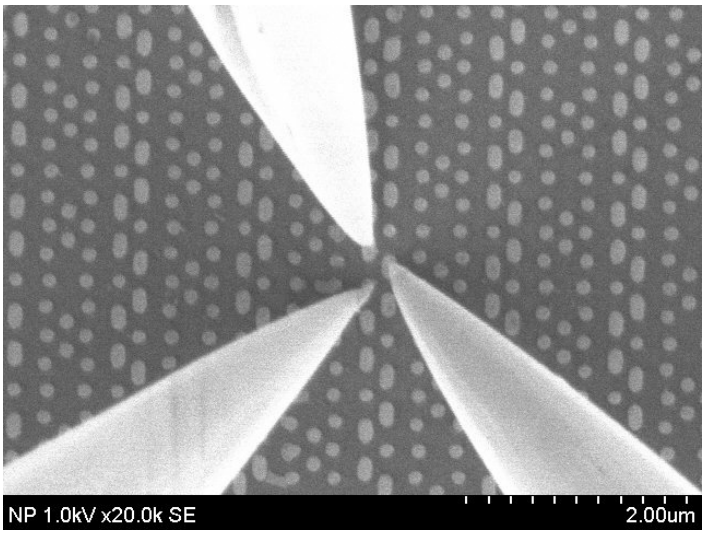


Fig. 3-18 Probing Image

* EBAC is described hereafter.

② Probing using an atomic force microscope (AFM)

Devices that scan the sample surface using a probe that is sharp at the atomic level and measure surface shapes and electron states at the atomic level are collectively known as scanning probe microscopes (SPM), and there are various types of SPM according to the physical quantity of the detection subject. Of the different types, atomic force microscopes (AFM) use a microscopic flat spring called a cantilever as the probe, and scan while contacting the sample surface. The cantilever displacement due to the sample surface condition is detected to obtain the AFM image.

In addition to the previously described SEM prober, the Sony Semiconductor Business Unit also currently has an AFM prober, and can obtain the electrical characteristics of elements by probing wiring and contacts with the cantilever based on the acquired AFM image. This is used to evaluate the characteristics of analog products in particular. (See Fig. 3-19.)

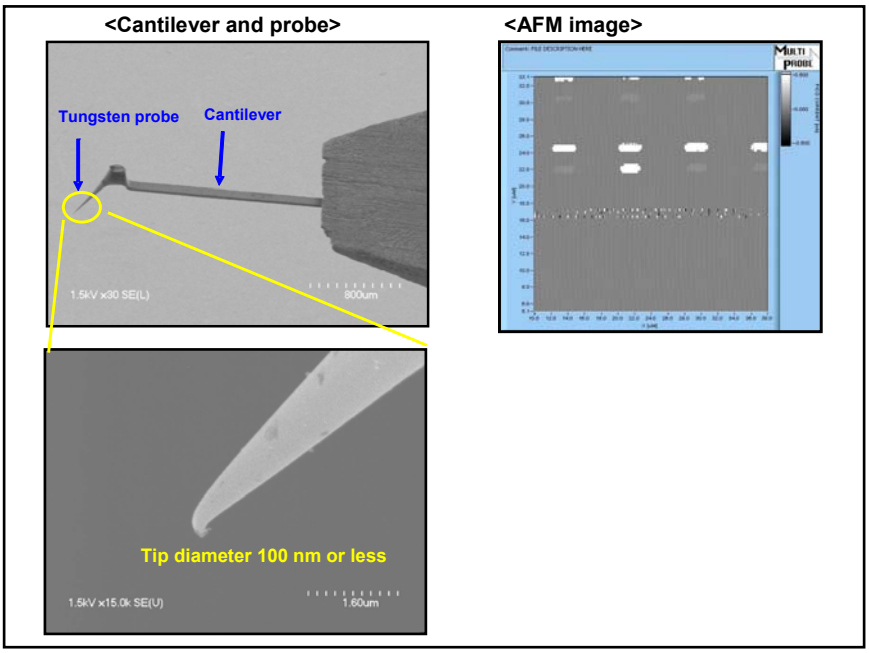


Fig. 3-19 AFM Image

(3) EBAC technology

As semiconductor device elements become more miniaturized and wiring layers increase, failures rooted in the wiring via holes that connect each layer are also increasing. In addition, wiring via hole defects are difficult to narrow down by existing analysis methods such as emissions analysis and IR-OBIRCH, and often cannot be confirmed by two-dimensional observation using layer removal analysis. Therefore, effective analysis methods are required.

EBAC is an effective analysis method for the above-mentioned wiring via hole open connection and high-resistance failures, and uses the current absorbed by the metal wiring (= absorbed current) when a device is irradiated by an electron beam. The equipment principle is as follows. The subject device is irradiated with an electron beam in the condition while directly probing a specific wiring or contact location with a highly accurate mechanical probe that uses an SEM prober. The generated absorbed current passes through the probe, is amplified by an amplifier, and the equipotential path is displayed as the absorbed current image. When open wiring connections or high-resistance locations are present, bright-dark contrast appears in the absorbed current image with those locations as the borders, enabling determination of failure locations. (See Fig. 3-20.) In principle, the detection sensitivity increases together with the resistance, but probing method and amplifier improvements currently enable detection of even low-resistance failures around 100 Ω.

The electron beam diameter expands and spatial resolution drops as the beam injection depth increases. Therefore, the practical EBAC analysis depth is two to three layers from the uppermost layer, and analysis of

lower layers requires removal of the upper layers. Alternately performing EBAC and layer removal analysis in this manner establishes an analysis method that identifies failure locations by a combination of electrical and physical analysis.

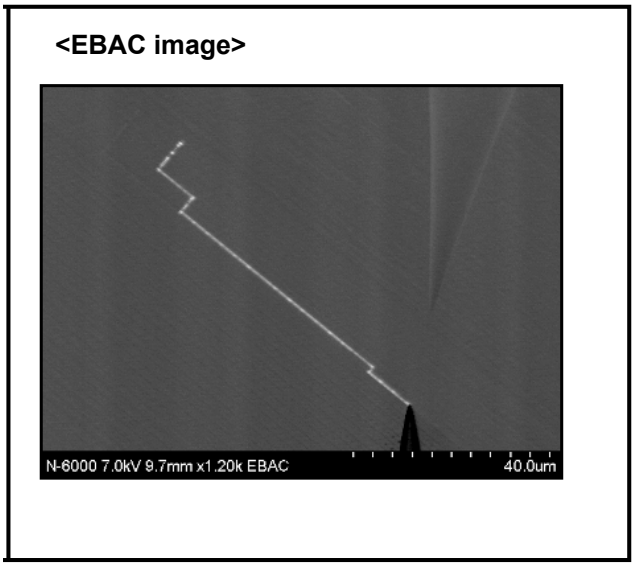


Fig. 3-20 EBAC Image

3.3.8 Chip Physical Analysis Technology

3.3.8.1 Description

In semiconductor device failure analysis, various analysis methods are first used to narrow down the failure location, and finally chip physical analysis technology is used to directly observe the failure location. Even when time is taken to narrow down a failure location, if physical analysis fails, ultimately no information can be obtained, so this is extremely important technology. However, while some cases can be clearly determined such as adherence of foreign matter or pattern damage, there are also cases where failures are not found even when physical analysis is performed.

Cases where failures are not be found are thought to mainly include the following:

1) The failure location was not properly narrowed down, and the failure is located in a different place.

2) The failure location was sufficiently narrowed down, but:

   ① The trouble was overlooked during physical analysis.

   ② An improper physical analysis method was selected (incorrect selection as to whether planar removal analysis or cross-sectional analysis is best), so the trouble could not be observed.

   ③ The trouble is of a level that cannot be physically observed (insufficient gate oxide film withstand voltage, crystal defect, etc.).

In these cases, the failure cause cannot be determined only by the skill of the physical analysis engineer. In addition, how far the range can be narrowed down in the isolation stage and how to select the analysis method (planar approach, cross-sectional approach, etc.) after isolating the range are extremely important factors, and affect the subsequent clarification rate.

The Sony Semiconductor Business Unit works to improve the failure cause clarification rate by ensuring constant coordination between engineers in various fields involved with failure analysis, selecting the optimum methods for isolating the failure location, and performing thorough physical analysis.

The technologies used to perform physical analysis on individual chips are introduced below.

3.3.8.2 Interlayer Removal Technology

After failure locations have been narrowed down using various analysis methods, the wiring layers and interlayer insulation film that form the circuits must be delaminated one layer at a time in order to physically observe the failures using SEM or other methods. The typical processing methods for this are as follows.

(1) Wet Etching

- Wiring layers, interlayer insulation film, and other items are etched away using chemicals.
- Use of chemicals suited to the materials provides good selectivity, but wet etching is isotropic etching

(etching progresses in both the vertical and horizontal directions), so it is difficult to apply to microscopic processes.

(2) Dry Etching

- This etching method uses the physical and chemical reactions between a gas and a solid (the material to be processed). A typical method is reactive ion etching (RIE).
- Dry etching is anisotropic etching (etching progresses in only one direction), so microscopic processing is possible.

(3) Surface Polishing

- This method indiscriminately removes all kinds of materials using a surface polisher and abrasives. The sample surface can be polished to a flat finish.

Recent semiconductor devices use a flattening process (chemical mechanical polishing: CMP) and a copper wiring process, so interlayer insulating films are mainly delaminated using dry etching, and wiring layers are mainly delaminated using surface polishing.

3.3.8.3 Chip Front and Rear Surface Observation Analysis

The observation equipment used to actually discover failure causes includes stereoscopic microscopes, metallographic microscopes, infrared microscopes, electron microscopes and other equipment in accordance with the purpose (size of observation subject, location to be observed, etc.). Stereoscopic microscopes are mainly used to observe the exterior of packages and other items, and metallographic microscopes are mainly used to observe chip surfaces, etc. In addition, infrared microscopes enable observation through silicon, so they are used for observation from the rear surface of the chip without performing exfoliation, such as when protective circuit breakdown is suspected. Theoretically, optical microscopes have submicron level resolution, but the actually observable level is such that they are used to observe trouble on a level of several microns. However, unlike electron microscopes, there is no need for a large-scale apparatus or preprocessing of samples, which means that optical microscopes are easy to use. As a result, they are used for “pre-observation” before observation using an electron microscope during failure analysis.

Stereoscopic microscopes, metallographic microscopes and infrared microscopes are called optical microscopes because they irradiate light (visible light or infrared light) at the sample for observation. In contrast, as the name implies, electron microscopes perform observation by irradiating electrons at the sample. The advantage of electron microscopes is a resolution that enables observation of objects at the atomic level. However, the apparatus is large scale, expensive (several hundred thousand to millions of dollars), and requires a special room that is not subject to magnetic fields, vibrations and other interference. Furthermore, some samples require preprocessing or other preparations, so some time is required before observation can be performed.

Electron microscopes are broadly classified into the following two types:

1) Scanning electron microscopes (SEM)

2) Transmission electron microscopes (TEM)

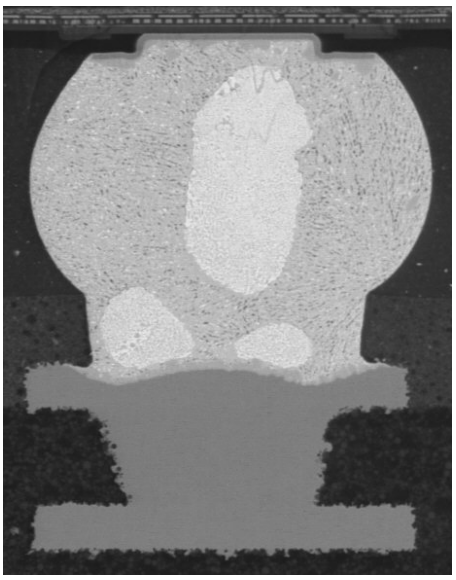
SEM used for surface observation are described below. TEM are described in a separate section.

3.3.8.3.1 Scanning Electron Microscope (SEM)

SEM performs observation by irradiating samples with an electron beam to generate reflected electrons, secondary electrons and characteristic X-rays. Of these, the reflected electrons and secondary electrons are collected by a detector, and that information is used to create images. The reflected electrons can be used to obtain a composition image, and the secondary electrons can be used to obtain a surface unevenness image. (See Fig. 3-21.) The remaining characteristic X-rays can also be used to analyze the constituent elements by EDX or other means. SEM is mainly used to observe planar removal samples. In addition, during SEM observation, metal objects connected to GND appear bright, and floating metal objects and insulating film appear dark (see Fig. 3-22), so SEM can also be used for the voltage contrast (VC) analysis method.

Semiconductor devices use insulating film (SiO_2, etc.) in locations other than the wiring materials. Therefore, if the electron beam is irradiated continuously for a long time during observation, the device becomes charged, preventing observation of clear images and causing burning and other various problems for continued analysis. For this reason, observation should be finished quickly in the minimum time necessary, or charging should be prevented by coating the surface of samples with carbon, gold or other conductive substances.

<Reflected electron image of solder bump>



<Secondary electron image of solder bump>

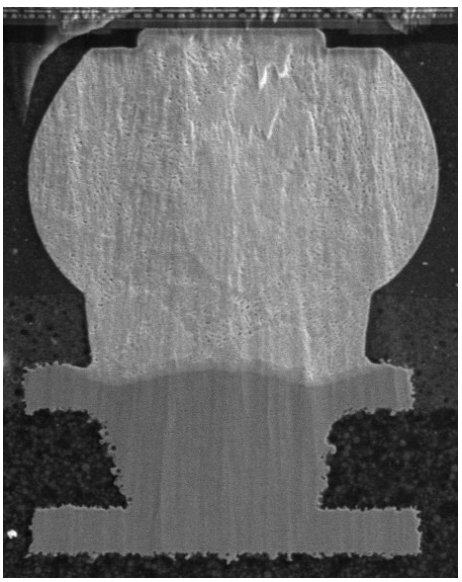


Fig. 3-21 Reflected Electron Image and Secondary Electron Image

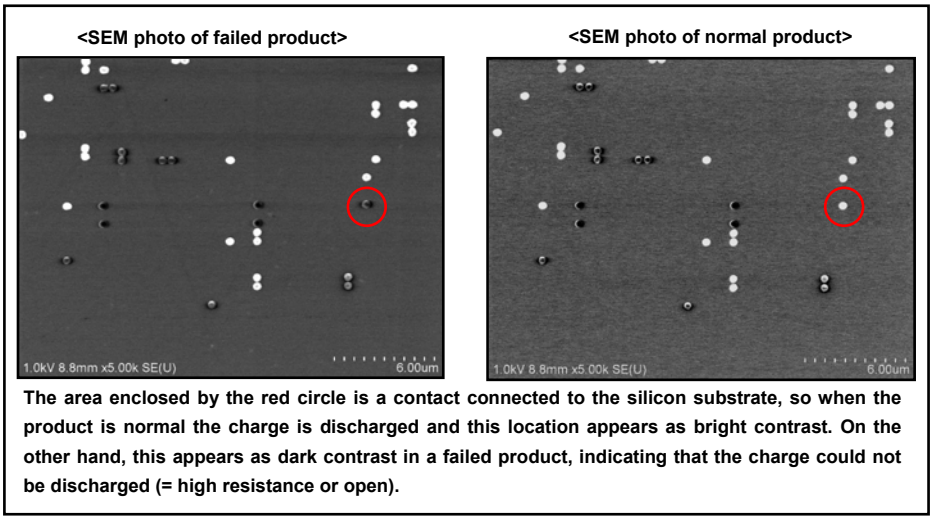


Fig. 3-22 VC Method Photo

3.3.8.4 Cross-sectional Analysis Technology

Cross-section samples for chip cross-section observation are mainly prepared using FIB. In addition, TEM is used for detailed observation of the prepared sample cross-sections. A thin slice of the area to be observed is created using FIB, picked up by the micro-sampling method, and set in a TEM holder, and the cross-section is then observed in detail using TEM. FIB and TEM are described below.

3.3.8.4.1 FIB

Gallium (Ga) is mainly used as the ion source, and the ions are accelerated by an electric field to create an ion beam that irradiates the surface of the sample. The required area can be etched by bumping out the surface atoms with the beam. The beam can be tightly focused to a diameter of several hundred nm to enable submicron level etching. As an additional function, FIB can also be used to vapor-deposit conductive films and insulating films. In addition to processing for cross-sectional analysis, this function can be used to repair semiconductor circuit wiring, making it possible to create bug-corrected samples of development products in a short time. A scanning ion microscope (SIM) can also be simultaneously used to enable easy observation of the sample cross-section during the above-mentioned etching or vapor deposition. In the SIM image, metal wiring connected to GND appears bright, and floating metal wiring and insulating film appear dark, so this can also be used for the VC analysis method in the same manner as SEM observation. However, during observation the Ga ions constantly strike the sample surface and etch the observed location, so observation must be performed as swiftly as possible.

3.3.8.4.2 TEM

TEM perform observation by irradiating a sample with an electron beam, collecting the electrons that pass through the sample with a detector located on the opposite side of the sample, and converting that information into an image. The transmitted electron beam level varies according to the components comprising the sample, so that information can be visualized to observe the sample structure. Therefore, TEM are mainly used to observe cross-sections. (See Fig. 3-23.)

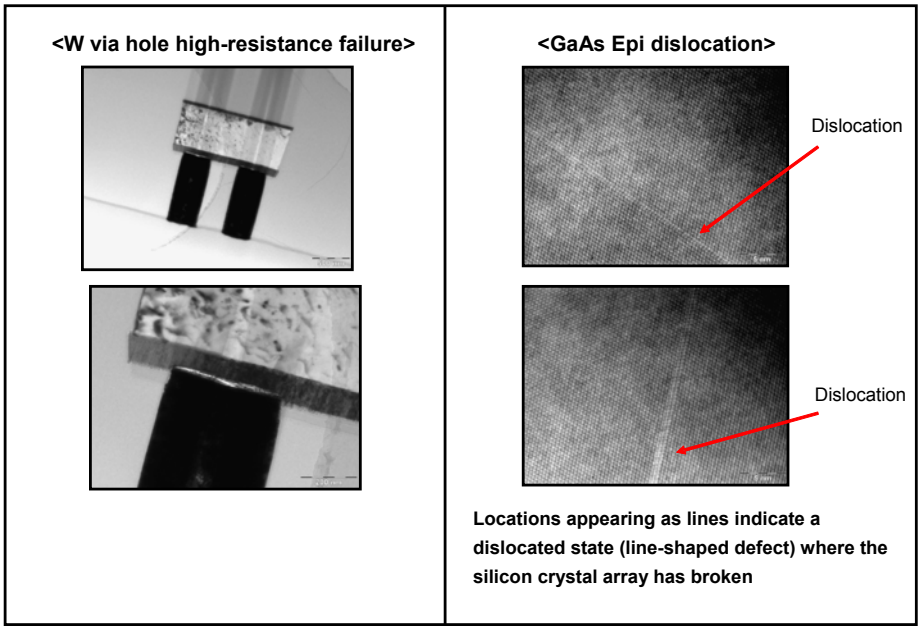


Fig. 3-23 TEM Images

However, in order for the electrons to pass through the sample, accelerated electrons must be transmitted at an ultra-high voltage (approximately 100 kV to 1000 kV). This means that a large apparatus (total length approximately 2 m to 8 m) is needed to obtain the acceleration voltage, so installation locations are limited, which is a disadvantage. Recently, even thinner samples can be machined using the above-mentioned FIB or other means, and technology (Ar milling) to remove damaged layers and achieve a flat finish during FIB processing is also advancing, so electrons can be transmitted at lower acceleration. In addition, scanning transmission electron microscopes (STEM) that combine both SEM and TEM functions are also often used.

3.3.9 Analysis Technologies

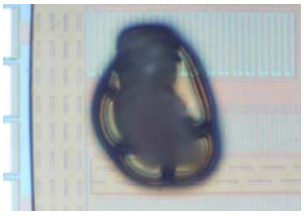
3.3.9.1 Description

When failure analysis is performed on a semiconductor device, various trouble may be confirmed, such as adherence of foreign matter or discoloration of metal wiring materials. Analysis technologies are used to identify these elements and materials, clarify the processes causing the trouble, and improve these processes.

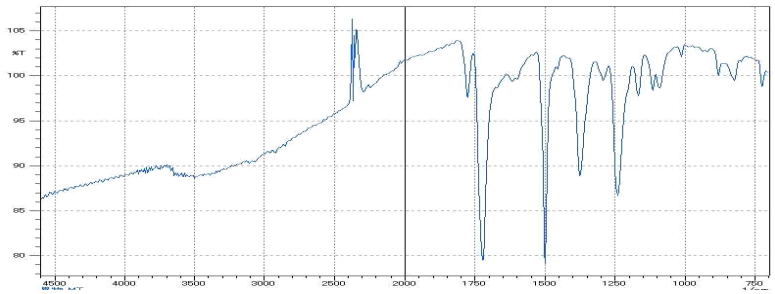
There are various types of analysis equipment, and the equipment most often used for failure analysis of semiconductor devices is described below.

3.3.9.2 Fourier Transform Infrared Spectroscopy (FT-IR) Analysis

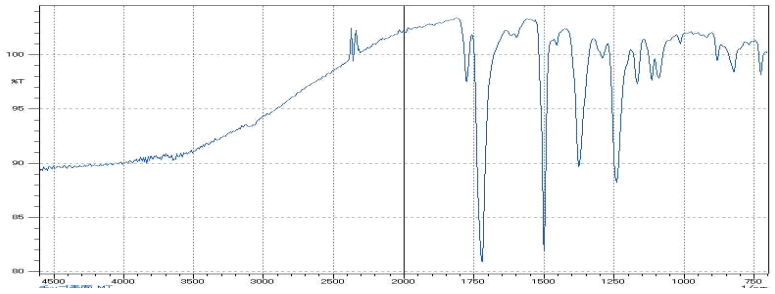
This analysis method is a measurement method that uses the infrared absorption of compound molecules when substances are irradiated by infrared rays to obtain information on the atomic bonding states of organic foreign matter. The functional groups contained in the measured object are understood from the obtained spectrum, enabling identification of the substance. Components can be easily determined by comparison with the spectrum in a database of known materials. In addition, measurement is performed in air, so solids, liquids and gases can be qualitatively and quantitatively analyzed. (See Fig. 3-24.)



Foreign matter adhered to wafer surface



FT-IR analysis results of adhered matter



FT-IR analysis results of polyimide (wafer surface)

Fig. 3-24 Examples of FT-IR Analysis (Example of Comparison with Known Materials)

When performing semiconductor device failure analysis, foreign matter is extremely small, so it is measured by the microscopic reflection and microscopic transmission methods using microscopes. When foreign matter has adhered to a bonding pad, land or other metal item, the microscopic reflection method that enables non-destructive measurement is mainly used. When foreign matter has adhered to the board or other organic substance, a sample is taken, and then the microscopic transmission method is used. Note that the minimum analysis area for these methods is approximately 15μm × 15μm.

In addition, the attenuated total reflectance (ATR) method is also a reflection method, and this method measures only the surface layer (approximately 1 μm) of a solid. This method contacts a crystal to the sample, so it cannot be used with non-flat samples, and it is also limited to subjects with an analysis area of approximately 100 μm x 100 μm or more. Note that non-destructive analysis can be performed, so measurement that maintains the trouble state is possible. In addition, the surface layer can be analyzed, so for example component data can be obtained for both surfaces of tapes.

FT-IR analysis allows easy analysis, and extensive databases are available, making it the most effective method especially for identification of organic compounds. However, the sensitivity is relatively low. It is said that a content of approximately 10% or more is required for detection, and this method is not suitable for analysis of microscopic areas of several μm or less in diameter or minute quantities such as contamination.

3.3.9.3 Energy Dispersive X-ray Spectrometer (EDX) and Wavelength Dispersive X-ray Spectrometer (WDX) Analysis

These analysis methods can identify atomic elements by irradiating an extremely tightly focused electron beam to the analysis subject (solid) and measuring the characteristic X-rays generated at that time with a detector. In addition, the element quantities contained in the sample can also be measured. Elements are detected to a depth of several microns, so these methods are unsuitable for analysis of only the uppermost surface layers. There are two types of analysis methods as follows according to the difference in detection methods.

1) EDX (energy dispersion analysis): This analysis method amplifies all of the generated specific X-rays using a semiconductor detector, and distributes the X-ray wavelengths by energy.

2) WDX (wavelength dispersion analysis): This analysis method uses X-ray analysis crystals with arbitrarily set wavelengths to sort the generated specific X-rays and analyze the selected the X-rays.

Each method has advantages and disadvantages. EDX has a lower wavelength resolution compared to WDX, but multiple elements can be analyzed simultaneously, so qualitative analysis can be performed in a short time. The lower wavelength resolution means that adjacent peaks often overlap, so the data must be carefully interpreted to avoid incorrect judgments. In addition, EDX is not suited to analysis of lighter elements.

WDX has better wavelength resolution compared to EDX, and there is little overlap between adjacent peaks, which eliminates identification mistakes. WDX uses analysis crystals to identify a single element with a single channel, so microscopic element amounts (approximately 10 ppm) can be analyzed, and lighter elements that cannot be detected by EDX are also covered. On the other hand, there is the demerit that the analysis time increases.

When performing actual analysis, the above characteristics are used to roughly analyze the approximate element configuration in a short time by EDX, and then WDX is used to confirm the identification results and perform detailed analysis of the target elements. (See Fig. 3-25 and Fig. 3-26.)

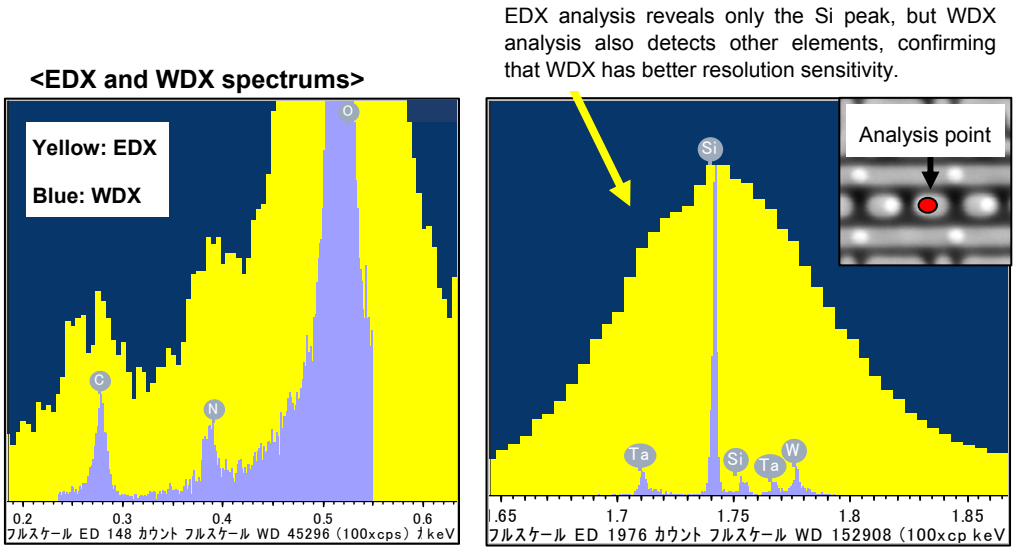
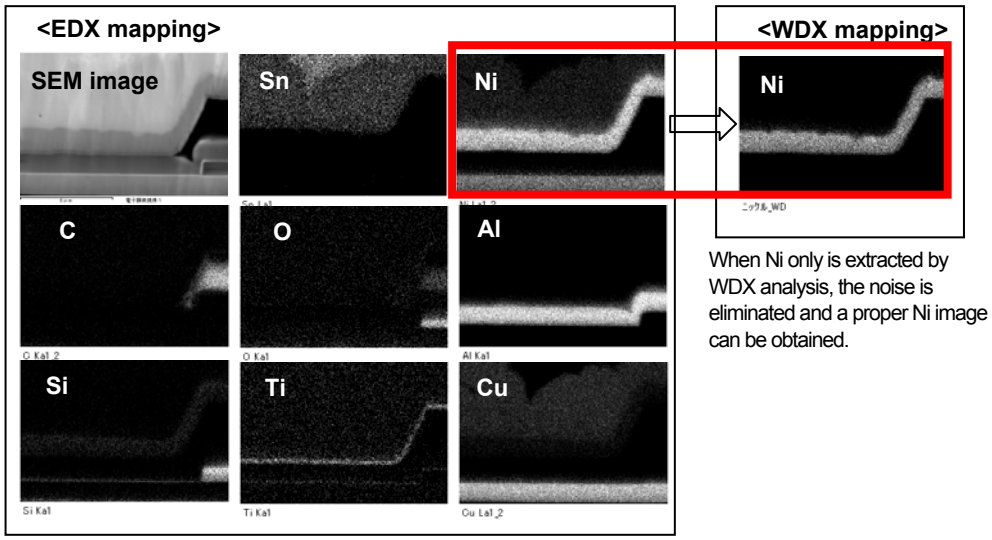


Fig. 3-25 Example of EDX and WDX Analysis



EDX analysis can analyze multiple elements simultaneously in a short time.
However, the peak resolution is poor and susceptible to noise, so accurate element distributions cannot be confirmed in some cases. (The above example uses Ni.)

Fig. 3-26 Example of EDX and WDX Analysis

3.3.9.4 Auger Electron Spectroscopy (AES) Analysis

This analysis method can identify elements with ultra-high sensitivity by irradiating an extremely tightly focused electron beam to the analysis subject (solid) and detecting the spectrum of the Auger electrons generated from the uppermost surface layers (up to several nm from the surface) of the subject at that time. In addition, the element quantities contained in the sample can also be measured.

Etching can also be performed using argon ions, which enables confirmation of the element distribution in the depth direction (depth-profile) and also the extent of trouble range and progression of contamination, etc. (See Fig. 3-27.)

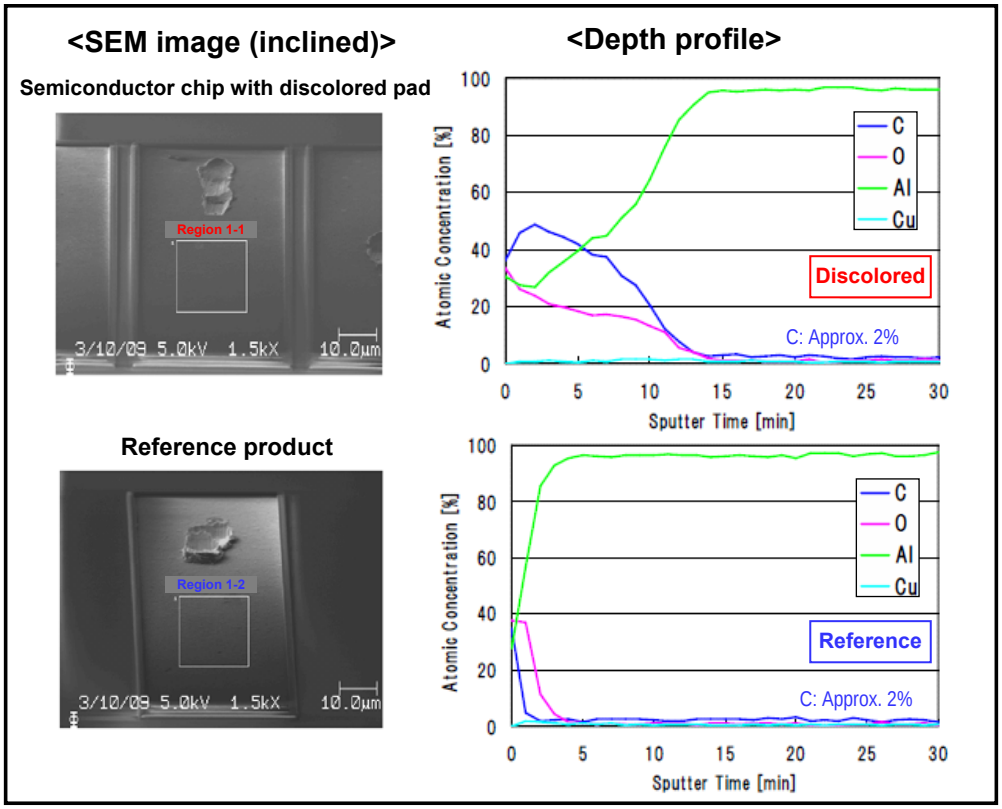


Fig. 3-27 Example of AES Analysis

In semiconductor device failure analysis, AES is used in particular to analyze foreign matter, discoloration and corrosion of bonding pads, metal wiring and other metal items, and thin film contamination, etc.

3.3.10 Confirmation of Relation between Trouble and Failure Mechanisms

When failure analysis is performed, it is important to be able to describe the trouble determined at that time as having reliably caused the failure. This is because many cases of “trouble” are not necessarily causes of failure.

For example, even when a wiring pattern is found to have an abnormal shape, unless there is actual contact with adjacent wiring or other functional trouble, it can be said to not look good, but it cannot be said to be the cause of the trouble. In these cases there is always some other true cause of the trouble, and that true cause must be reliably found to lead to proper improvement.

In this manner, when trouble is confirmed using various analysis methods, it must be possible to explain that the trouble is consistent with the trouble symptoms and electrical characteristics. Only when this can be explained can it be said that the failure cause has been determined. However, as a result of recent increases in semiconductor device integration and circuit scale, trouble symptoms are also becoming more complex, and this is making it difficult for analysis technology engineers alone to confirm whether trouble symptoms and failure causes match.

In the Sony Semiconductor Business Unit, circuit design engineers, product technology engineers, reliability technology engineers, process engineers and others all cooperate to reliably clarify failure mechanisms, implement the appropriate improvements, and conduct continuous quality improvement activities.